SIGNAL PROCESSING TECHNOLOGIES

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1991-1992 PRODUCT CATALOG

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GENERAL INFORMATION

TYPES OF DATA SHEETS

ADVANCE INFORMATION — These data sheets contain the descriptions of products that are in development. The specifications are based on engineering calculations, computer simulations and/or initial prototype evaluation.

PRELIMINARY — These data sheets contain minimum and maximum specifications that are based on initial device characterization. These limits are subject to change upon the completion of full characterization over the specified temperature and supply voltage ranges.

FINAL — These data sheets contain specifications based on complete characterizations of the devices over the specified temperature and supply voltage ranges.

WARRANTY

SPT warrants that standard products (except for board-level products) delivered hereunder shall be free from defects in material and workmanship under normal use and service for a period of one (1) year from the date of shipment from SPT's facility. Board level products delivered hereunder shall be free from defects in material and workmanship under normal use and service for a period of ninety (90) days from the date of shipment from SPT's facility. For products which are not standard products, such as dice and wafers, SPT warrants to Buyer that such products shall be free from defects in material and workmanship under normal use and service for a period of thirty (30) days from the date of shipment. Products which are "engineering samples" are sold AS IS, "WITH ALL FAULTS," and with no warranty whatsoever.

If, during such one year, ninety day or thirty-day period (i) SPT is notified promptly in writing upon discovery of any defect in the goods, including a detailed description of such defect; (ii) such goods are returned to SPT, F.O.B. SPT's facility; and (iii) SPT's examination of such goods discloses to SPT's satisfaction that such goods are defective and such defects are not caused by accident, abuse, misuse, neglect, alteration, improper installation, repair or alteration by someone other than SPT, improper testing, or use contrary to any instructions issued by SPT, within a reasonable time, SPT shall (at its sole option) either replace or credit Buyer the purchase price of such goods.

Prior to any return of goods by Buyer pursuant to the section, Buyer shall afford SPT the opportunity to inspect such goods at Buyer's location, and any such goods so inspected shall not be returned to SPT without its prior written consent.

SPT shall return any goods repaired or replaced under this warranty to Buyer, transportation prepaid, and reimburse Buyer for the transportation charges paid by Buyer for such goods. The performance of this warranty does not extend the warranty period for any goods beyond that period applicable to the goods originally delivered.

The foregoing warranty constitutes SPT's exclusive liability, and the exclusive remedy of Buyer, for any breach of any warranty or other nonconformity of the goods covered by this quotation. THIS WARRANTY IS EXCLUSIVE, AND IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE, WHICH ARE HEREBY EXPRESSLY DISCLAIMED.

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LIFE SUPPORT APPLICATIONS POLICY

WARNING — Signal Processing Technologies' products shall not be used within any life support systems without the specific written consent of Signal Processing Technologies. A life support system is a product or system intended to support or sustain life which, if it fails, can be reasonably expected to result in a significant personal injury or death.

TABLE OF CONTENTS

PRODUCT SELECTION GUIDE

A/D CONVERTERS

PART NO.	GRADES	RESOLUTION (BITS)	SAMPLE RATE (MSPS)	INL (LSB)/ SNR (dB)	POWER (WATTS)	TEMP RANGE	PKGS/ PINS	QUAL LEVEL	FEATURES
HIGH SPEED									
HADC77100	A	8	150	1/2	<2.2	I, M	J / 42	/H	PREAMPLIFIER DESIGN
	B			3/4		I			
HADC77200	A	8	150	1/2	<2.2	I, M	J / 48	/H	DATA READY AND OVERRANGE OUTPUTS, QUARTER POINT LADDER TAPS
	B			3/4	<2.2	I			
SPT7810	A	10	20	59	1.3	I	J / 28	*	ON-CHIP TRACK/HOLD MONOLITHIC
	B			56					
SPT7814	A	10	40	57	1.3	I	J / 28	*	ON-CHIP TRACK/HOLD MONOLITHIC
	B			54				*	
SPT7820	-	10	20	59	1.0	I	J / 28	*	TTL OUTPUT VERSION OF SPT7810
SPT7824	-	10	40	57	1.0	I	J / 28	*	TTL OUTPUT VERSION OF SPT7814
SPT7910	-	12	10	68	1.4	I	J / 32	*	INCLUDES S/H ON MONOLITHIC DIE
SPT7912	-	12	20	68	1.4	I	J / 32	*	INCLUDES S/H ON MONOLITHIC DIE
SPT7920	-	12	10	68	1.1	I	J / 32	*	TTL OUTPUT VERSION OF SPT7910
SPT7922	-	12	20	68	1.1	I	J / 32	*	TTL OUTPUT VERSION OF SPT7912

*CONSULT FACTORY FOR AVAILABILITY OF MILITARY TEMPERATURE RANGE AND /883 PROCESSED UNITS.

PRODUCT SELECTION GUIDE

A/D CONVERTERS (Continued)

PART NO.	GRADES	RESOLUTION (BITS)	CONVERSION TIME (µsec)	LINEAR-ITY (LSB)	INPUT RANGES (V)	TEMP RANGE	PKGS / PINS	QUAL LEVEL	FEATURES
SPT7572	A	12	5/12	1/2	0-5	C	J / 24	-	IMPROVED INPUT CIRCUITRY
	B			1					
	C			1					
SPT774	A	12	8	1/2	±5, ±10	C, I, M	J, D, C, U / 28	/883	MONOLITHIC, S/H FUNCTION, LOW POWER. ALTERNATIVE FOR HI774
	B			1/2	0-10, 0-20				
	C			1					
HADC674Z	A	12	15	1/2	±5, ±10	C, I, M	J, D, C, U / 28	/883	MONOLITHIC, S/H FUNCTION, LOW POWER, NO NEGATIVE SUPPLY REQUIRED, HI674 ALTERNATIVE
	B			1/2	0-10, 0-20				
	C			1					
HADC574Z	A	12	25	1/2	±5, ±10	C, I, M	J, D, C, U / 28	/883	MONOLITHIC, S/H FUNCTION, LOW POWER, NO NEGATIVE SUPPLY REQUIRED, ALTERNATIVES FOR HI574 AND AD574
	B			1/2	0-10, 0-20				
	C			1					

D/A CONVERTERS

PART NO.	GRADES	RESOLUTION (BITS)	GLITCH ENERGY (PV -S)	LINEAR-ITY (LSB)	CONVERSION RATE (MWPS)	TEMP RANGE	PKGS / PINS	QUAL LEVEL	FEATURES
ECL LOGIC									
HDAC51400	S	8	10	1/2	400	I/M	D/24	/883	REF, VIDEO CONTROL
HDAC10181	A	8	10	1/2	275	I/M	D / 24	/883	REF, VIDEO CONTROL
	B			1/2	165				
HDAC10180	A	8	10	1/2	275	I/M	D / 24	/883	VIDEO CONTROL ALTERNATIVE FOR TDC1018
	B			1/2	165				

PRODUCT SELECTION GUIDE

D/A CONVERTERS (Continued)

PART NO.	GRADES	RESOLUTION (BITS)	SETTLING TIME (ns)	LINEAR-ITY (LSB)	OUTPUT TYPE	TEMP RANGE	PKGS / PINS	QUAL LEVEL	FEATURES
TTL LOGIC									
HDAC7542A	A	12	500	1/2	I	C, I, M	N, D	-	ALTERNATIVE FOR
							/		AD7542
	B			1			16		
HDAC7543A	A	12	500	1/2	I	C, I, M	N, D	-	AD7543 ALTERNATIVE
							/		
	B			1			16		
HDAC7545A	A	12	500	1/2	I	C, I, M	N, D	-	ALTERNATIVE FOR
							/		AD7545
	B			1			20		
HDAC52160	A	16	150	1	I,V	I	J		PARALLEL INPUT,
							/		REFERENCE, OUTPUT
	B			2			32		RANGE: +10 to 0, +5 to 0,
									±5 OR ±2.5 V
	C			4					

COMPARATORS

PART NO.	GRADES	TR/TF (NS)	PROP DELAY (NS)	V_{CM} (V)	V_{OS} (V)	POWER DISSIPATION (mW)	TEMP RANGE	PKGS / PINS	FEATURES
HCMP96850	S	1.76/1.76	2.4	±2.5	±3.0	125	I	D, U	SYMMETRICAL TR/TF,
								/	ALTERNATE FOR SP9685,
								16	AM6685, AD9685
HCMP96870/A	S	1.2/1.2	2.0	±2.5	±3.0	250	I	N, J, D, C, P	HIGH PERFORMANCE,
								/	ALTERNATE FOR SP9687,
								16,16,16,20,20	AM6687, AD9687
SPT9689	A	.18/.08	.65	-2.5/+4.0	±10	350	I	J/C	900 MHz BANDWIDTH
								/	DIFFERENTIAL LATCH CONTROL
	B				±25			16/20	

PRODUCT SELECTION GUIDE

FILTERS

PART NO.	GRADES	DYNAMIC RANGE (dB)	MAX BANDEDGE (kHz)	BANDEDGE TOLERANCE (%)	SUPPLY VOLTAGE (V)	TEMP RANGE	PKGS / PINS	FEATURES
HSCF24040	A	85	20	±0.5	±5.0	C, M	J, C / 32, 28	7th ORDER LOW PASS, >76 dB STOPBAND ATTENUATION, ON-CHIP ANTI-ALIAS FILTER, DIGITALLY PROGRAMMABLE BANDEDGE AND DC

VOLTAGE REGULATORS

PART NO.	OUTPUT VOLTAGE (V)	OUTPUT VOLTAGE REGULATION (%)	OUTPUT CURRENT (ma)	DROPOUT VOLTAGE (mV)	OUTPUT NOISE (μV_{RMS})	FEATURES
SPT114	2.0 to 8.0 (11 Versions)	±3.5	70	120	180	ON/OFF SWITCH; SHORT CIRCUIT PROTECTION
SPT115	2.5 to 8.0 (10 Versions)	±3	100	170	180	ON/OFF SWITCH; SHORT CIRCUIT PROTECTION
SPT116	2.0 to 5.5 (8 Versions)	±3	100	50	150	THREE TERMINAL; THERMAL SHUTDOWN

DC/DC CONVERTERS

PART NO.	OUTPUT VOLTAGE (V)	INPUT VOLTAGE (V)	OUTPUT CURRENT (ma)	FEATURES
SPT11806	9.3 to 32	1.1 to 18	0.1	BUILT-IN VOLTAGE REFERENCE AND RELAXATION OSCILLATOR
SPT11821	10 to 24	0.9 to 10.0	2.4	BUILT-IN OSCILLATOR AND SMALL SURFACE MOUNT PACKAGE

PRODUCT CROSS REFERENCE GUIDE

(INDUSTRIAL SPT EQUIVALENT)

AMD	SPT	DESCRIPTION
AM6685DL	HCMP96850SID	SINGLE COMPARATOR
AM6687DL	HCMP96870SID/A	DUAL COMPARATOR
AM6687LL	HCMP96870SIC/A	DUAL COMPARATOR

ANALOG DEVICES	SPT	DESCRIPTION
AD574AJD	HADC574ZCCD	12-BIT ADC
AD574AKD	HADC574ZBCD	12-BIT ADC
AD574ALD	HADC574ZACD	12-BIT ADC
AD574ASD	HADC574ZCMD	12-BIT ADC
AD574ATD	HADC574ZBMD	12-BIT ADC
AD574AUD	HADC574ZAMD	12-BIT ADC
AD674AJD	HADC674ZCCD	12-BIT ADC
AD674AKD	HADC674ZBCD	12-BIT ADC
AD674ALD	HADC674ZACD	12-BIT ADC
AD674ASD	HADC674ZCMD	12-BIT ADC
AD674ATD	HADC674ZBMD	12-BIT ADC
AD674AUD	HADC674ZAMD	12-BIT ADC
AD1674	SPT774	12-BIT ADC
AD7542ACHIPS	HDAC7542ACCU	12-BIT DAC
AD7542AD	HDAC7542ABID	12-BIT DAC
AD7542BD	HDAC7542AAID	12-BIT DAC
AD7542GBD	HDAC7542AAID/G	12-BIT DAC
AD7542GTD	HDAC7542AAMD/G	12-BIT DAC
AD7542SD	HDAC7542ABMD	12-BIT DAC
AD7542TD	HDAC7542AAMD	12-BIT DAC
AD7542GKN	HDAC7542AACD/G	12-BIT DAC
AD7542KN	HDAC7542AACD	12-BIT DAC
AD7542JN	HDAC7542ABCD	12-BIT DAC
AD7543ACHIPS	HDAC7543ACCU	12-BIT DAC
AD7543AD	HDAC7543ABID	12-BIT DAC
AD7543BD	HDAC7543AAID	12-BIT DAC
AD7543GBD	HDAC7543AAID/G	12-BIT DAC
AD7543GTD	HDAC7543AAMD/G	12-BIT DAC
AD7543SD	HDAC7543ABMD	12-BIT DAC
AD7543SD	HDAC7543ABMD	12-BIT DAC
AD7543TD	HDAC7543AAMD	12-BIT DAC
AD7543GKN	HDAC7543AACD/G	12-BIT DAC
AD7543KN	HDAC7543AACD	12-BIT DAC
AD7543JN	HDAC7543ABCD	12-BIT DAC

ANALOG DEVICES	SPT	DESCRIPTION
AD7545ACHIPS	HDAC7545ACCU	12-BIT DAC
AD7545AQ	HDAC7545ABID	12-BIT DAC
AD7545BQ	HDAC7545ABID	12-BIT DAC
AD7545CQ	HDAC7545AAID	12-BIT DAC
AD7545GCQ	HDAC7545AAID/G	12-BIT DAC
AD7545GUD	HDAC7545AAMD/G	12-BIT DAC
AD7545SD	HDAC7545ABMD	12-BIT DAC
AD7545TD	HDAC7545ABMD	12-BIT DAC
AD7545UD	HDAC7545AAMD	12-BIT DAC
AD7545GLN	HDAC7545AACD/G	12-BIT DAC
AD7545LN	HDAC7545AACD	12-BIT DAC
AD7545KN	HDAC7545ABCD	12-BIT DAC
AD7545JN	HDAC7545ABCD	12-BIT DAC
AD7572JN05	SPT7572CCJ/05	12-BIT ADC
AD7572KN05	SPT7572BCJ/05	12-BIT ADC
AD7572LN05	SPT7572ACJ/05	12-BIT ADC
AD7572JN12	SPT7572CCJ/12	12-BIT ADC
AD7572KN12	SPT7572BCJ/12	12-BIT ADC
AD7572LN12	SPT7572ACJ/12	12-BIT ADC
AD9685B	HCMP96850SID	SINGLE COMPARATOR
AD9687B	HCMP96870SID/A	DUAL COMPARATOR

BURR BROWN	SPT	DESCRIPTION
ADC574AJP	HADC574ZCCD	12-BIT ADC
ADC574AKP	HADC574ZBCD	12-BIT ADC
ADC574ASH	HADC574ZCMD	12-BIT ADC
ADC574ATH	HADC574ZBMD	12-BIT ADC
ADC674AJP	HADC674ZCCD	12-BIT ADC
ADC674AKP	HADC674ZBCD	12-BIT ADC
ADC674ASH	HADC674ZCMD	12-BIT ADC
ADC674ATH	HADC674ZBMD	12-BIT ADC
ADC774JP	SPT774CCJ	12-BIT ADC
ADC774KP	SPT774BCJ	12-BIT ADC
ADC774SH	SPT774CMJ	12-BIT ADC
ADC774TH	SPT774BMJ	12-BIT ADC

HARRIS	SPT	DESCRIPTION
HI1-574AJD-5	HADC574ZCCJ	12-BIT ADC
HI1-574AKD-5	HADC574ZBCJ	12-BIT ADC
HI1-574ALD-5	HADC574ZACJ	12-BIT ADC
HI1-574ASD-2	HADC574ZCMJ	12-BIT ADC
HI1-574ATD-2	HADC574ZBMJ	12-BIT ADC
HI1-574AUD-2	HADC574ZAMJ	12-BIT ADC

PRODUCT CROSS REFERENCE GUIDE

(INDUSTRIAL SPT EQUIVALENT)

HARRIS	SPT	DESCRIPTION
HI1-674AJD-5	HADC674ZCCJ	12-BIT ADC
HI1-674AKD-5	HADC674ZBCJ	12-BIT ADC
HI1-674ALD-5	HADC674ZACJ	12-BIT ADC
HI1-674ASD-2	HADC674ZCMJ	12-BIT ADC
HI1-674ATD-2	HADC674ZBMJ	12-BIT ADC
HI1-674AUD-21	HADC674ZAMJ	12-BIT ADC
HI1-774J-5	SPT774CCJ	12-BIT ADC
HI1-774K-5	SPT774BCJ	12-BIT ADC
HI1-774S-2	SPT774CMJ	12-BIT ADC
HI1-774T-2	SPT774BMJ	12-BIT ADC

MAXIM	SPT	DESCRIPTION
MAX663	*SPT114/115	VOLTAGE REGULATOR
MAX667	*SPT114/115	VOLTAGE REGULATOR
MX7572LN05	SPT7572ACJ/05	12-BIT ADC
MX7572KN05	SPT7572BCJ/05	12-BIT ADC
MX7572JN05	SPT7572CCJ/05	12-BIT ADC
MX7572LN12	SPT7572ACJ/12	12-BIT ADC
MX7572KN12	SPT7572BCJ/12	12-BIT ADC
MX7572JN12	SPT7572CCJ/12	12-BIT ADC

MICRO POWER	SPT	DESCRIPTION
MP7542DIE	HDAC7542ACCU	DIE
MP7542AD	HDAC7542ABID	12-BIT DAC
MP7542BD	HDAC7542AAID	12-BIT DAC
MP7542SD	HDAC7542ABMD	12-BIT DAC
MP7542TD	HDAC7542AAMD	12-BIT DAC
MP7543DIE	HDAC7543ACCU	DIE
MP7543AD	HDAC7543ABID	12-BIT DAC
MP7543BD	HDAC7543AAID	12-BIT DAC
MP7543SD	HDAC7543ABMD	12-BIT DAC
MP7543TD	HDAC7543AAMD	12-BIT DAC
MP7545DIE	HDAC7545ACCU	DIE
MP7545AD	HDAC7545ABID	12-BIT DAC
MP7545BD	HDAC7545AAID	12-BIT DAC
MP7545CD	HDAC7545AAID	12-BIT DAC
MP7545SD	HDAC7545ABMD	12-BIT DAC
MP7545UD	HDAC7545AAMD	12-BIT DAC

NATIONAL	SPT	DESCRIPTION
LM2931	SPT116	VOLTAGE REGULATOR
LM2931A	SPT116	VOLTAGE REGULATOR
LM2936	SPT116	VOLTAGE REGULATOR

PLESSEY	SPT	DESCRIPTION
SP9685DG	HCMP96850SID	SINGLE COMPARATOR
SP9687DG	HCMP96870SID/A	DUAL COMPARATOR

PMI/ADI	SPT	DESCRIPTION
PM7542AQ	HDAC7542AAMD/G	12-BIT DAC
PM7542BQ	HDAC7542AAMD	12-BIT DAC
PM7542BQ	HDAC7542ABMD	12-BIT DAC
PM7542EQ	HDAC7542AAID/G	12-BIT DAC
PM7542FQ	HDAC7542AAID	12-BIT DAC
PM7542FQ	HDAC7542ABID	12-BIT DAC
PM7542G	HDAC7542ACCU	DIE
PM7543AQ	HDAC7543AAMD/G	12-BIT DAC
PM7543BQ	HDAC7543AAMD	12-BIT DAC
PM7543BQ	HDAC7543ABMD	12-BIT DAC
PM7543EQ	HDAC7543AAID/G	12-BIT DAC
PM7543FQ	HDAC7543AAID	12-BIT DAC
PM7543FQ	HDAC7543ABID	12-BIT DAC
PM7543G	HDAC7543ACCU	DIE
PM7545AR	HDAC7545AAMD/G	12-BIT DAC
PM7545BR	HDAC7545AAMD	12-BIT DAC
PM7545BR	HDAC7545ABMD	12-BIT DAC
PM7545ER	HDAC7545AAID/G	12-BIT DAC
PM7545FR	HDAC7545AAID	12-BIT DAC
PM7545FR	HDAC7545ABID	12-BIT DAC
PM7545G	HDAC7545ACCU	DIE

SEIKO	SPT	DESCRIPTION
S-8850	*SPT114/115	VOLTAGE REGULATOR
S-812xxAG	SPT116	VOLTAGE REGULATOR
S-812xxHG	SPT116	VOLTAGE REGULATOR
S-812xxPG	SPT116	VOLTAGE REGULATOR
S-813xxHG	SPT116	VOLTAGE REGULATOR

SONY	SPT	DESCRIPTION
CX20116	HADC77100AIJ	8-BIT, 150MSPS ADC

TEXAS INST	SPT	DESCRIPTION
TL751LXD	*SPT114/115	VOLTAGE REGULATOR
TL751LXP	*SPT114/115	VOLTAGE REGULATOR
TL750LXD	*SPT116	VOLTAGE REGULATOR
TL750LXP	*SPT116	VOLTAGE REGULATOR
TL750LXLP	SPT116	VOLTAGE REGULATOR

TRW	SPT	DESCRIPTION
TDC1018	HDAC10180	8-BIT, 275MWPS DAC

* Functional Replacement

SPT PRODUCT IDENTIFICATION CODE

HADC 574Z A C D/ 883

- **HADC** — PREFIX
- **574Z** — PRODUCT NUMBER
- **A** — ELECTRICAL GRADE
- **C** — TEMPERATURE OPERATING RANGE
- **D/** — PACKAGE TYPE
- **883** — SPECIAL BY CUSTOMER DRAWING OR SCREEN

SPECIAL BY CUSTOMER DRAWING OR SCREEN (883)

Options:

B	Standard Burn-In
H	Standard Hi-Rel Screening
E	Special Electric
883	Compliant to /883 Standards

PACKAGE TYPE (D/)

J	Ceramic Sidebrazed
D	Cerdip
C	Leadless Chip Carrier
G	Pin Grid Array
N	Plastic Dip
P	Plastic Leaded Chip Carrier
U	Die

TEMPERATURE OPERATING RANGE (C)

M	Military (-55 to +125 °C)
I	Industrial (-25 to +85 °C)
C	Commercial (0 to +70 °C)

ELECTRICAL GRADE (A)

A, B, C — Increasing Grade (A highest)

S	Single Grade
xx	Regulator Product Designator

PRODUCT NUMBER (574Z)

(See Product Listings)

PREFIX (HADC)

ADC	Analog-to-Digital Converter
CMP	Comparator
DAC	Digital-to-Analog Converter
SCF	Switched Capacitor Filter
SPT	New SPT Products

ORDERING INFORMATION

ANALOG-TO-DIGITAL CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HADC574ZAC(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC574ZBC(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC574ZCC(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC574ZAI(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC574ZBI(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC574ZCI(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC574ZAM(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC574ZBM(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC574ZCM(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC574ZAM(X)/883	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC574ZBM(X)/883	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC574ZCM(X)/883	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC574Z	12-BIT, 25 µsec ADC	DIE		+25 °C
HADC674ZAC(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC674ZBC(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC674ZCC(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC674ZAI(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC674ZBI(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC674ZCI(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC674ZAM(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC674ZBM(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC674ZCM(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC674ZAM(X)/883	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC674ZBM(X)/883	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC674ZCM(X)/883	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC674Z	12-BIT, 15 µsec ADC	DIE		+25 °C
SPT774AC(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
SPT774BC(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
SPT774CC(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
SPT774AI(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT774BI(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT774CI(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT774AM(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY
SPT774BM(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY
SPT774CM(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY
SPT774AM(X)/883	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
SPT774BM(X)/883	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
SPT774CM(X)/883	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
SPT774	12-BIT, 8 µsec ADC	DIE	28	+25 °C
SPT7572ACJ/05	12-BIT, 5 µsec ADC	SIDEBRAZED	24	COMMERCIAL
SPT7572BCJ/05	12-BIT, 5 µsec ADC	SIDEBRAZED	24	COMMERCIAL
SPT7572CCJ/05	12-BIT, 5 µsec ADC	SIDEBRAZED	24	COMMERCIAL
SPT7572ACJ/12	12-BIT, 12 µsec ADC	SIDEBRAZED	24	COMMERCIAL
SPT7572BCJ/12	12-BIT, 12 µsec ADC	SIDEBRAZED	24	COMMERCIAL
SPT7572CCJ/12	12-BIT, 12 µsec ADC	SIDEBRAZED	24	COMMERCIAL

NOTE: (X) Denotes Package Type: J - SIDEBRAZED DIP; D - CERDIP; C - LCC

ORDERING INFORMATION

ANALOG-TO-DIGITAL CONVERTERS (Continued)

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HADC77100AIJ	8-BIT, 150 MSPS ADC ±1/2 LSB	SIDEBRAZED	42	INDUSTRIAL
HADC77100BIJ	8-BIT, 150 MSPS ADC ±3/4 LSB	SIDEBRAZED	42	INDUSTRIAL
HADC77100AMJ	8-BIT, 150 MSPS ADC ±1/2 LSB	SIDEBRAZED	42	MILITARY
HADC77100AMJ/H	8-BIT, 150 MSPS ADC ±1/2 LSB	SIDEBRAZED	42	MILITARY HI-REL
HADC77200AIJ	8-BIT, 150 MSPS ADC ±1/2 LSB	SIDEBRAZED	48	INDUSTRIAL
HADC77200BIJ	8-BIT, 150 MSPS ADC ±3/4 LSB	SIDEBRAZED	48	INDUSTRIAL
HADC77200AMJ	8-BIT, 150 MSPS ADC ±1/2 LSB	SIDEBRAZED	48	MILITARY
HADC77200AMJ/H	8-BIT, 150 MSPS ADC ±1/2 LSB	SIDEBRAZED	48	MILITARY HI-REL
SPT7810AI(X)	10-BIT, 20 MSPS ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT7810BI(X)	10-BIT, 20 MSPS ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT7810AM(X)	10-BIT, 20 MSPS ADC	SEE NOTE BELOW	28	MILITARY
SPT7810BM(X)	10-BIT, 20 MSPS ADC	SEE NOTE BELOW	28	MILITARY
SPT7810AM(X)/883	10-BIT, 20 MSPS ADC	SEE NOTE BELOW	28	MILITARY/883
SPT7810BM(X)/883	10-BIT, 20 MSPS ADC	SEE NOTE BELOW	28	MILITARY/883
SPT7810	10-BIT, 20 MSPS ADC	DIE	28	+25 °C
SPT7814AI(X)	10-BIT, 40 MSPS ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT7814BI(X)	10-BIT, 40 MSPS ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT7814AM(X)	10-BIT, 40 MSPS ADC	SEE NOTE BELOW	28	MILITARY
SPT7814BM(X)	10-BIT, 40 MSPS ADC	SEE NOTE BELOW	28	MILITARY
SPT7814AM(X)/883	10-BIT, 40 MSPS ADC	SEE NOTE BELOW	28	MILITARY/883
SPT7814BM(X)/883	10-BIT, 40 MSPS ADC	SEE NOTE BELOW	28	MILITARY/883
SPT7814	10-BIT, 40 MSPS ADC	DIE	28	+25 °C
SPT7820*	10-BIT, 20 MSPS, TTL, ADC	SIDEBRAZED, LCC	28	IND, MIL, /883
SPT7824*	10-BIT, 40 MSPS, TTL, ADC	SIDEBRAZED, LCC	28	IND, MIL, /883
SPT7910*	12-BIT, 10 MSPS, ECL, ADC	SIDEBRAZED	32	IND, MIL, /883
SPT7912*	12-BIT, 20 MSPS, ECL, ADC	SIDEBRAZED	32	IND, MIL, /883
SPT7920*	12-BIT, 10 MSPS, TTL, ADC	SIDEBRAZED	32	IND, MIL, /883
SPT7922*	12-BIT, 20 MSPS, TTL, ADC	SIDEBRAZED	32	IND, MIL, /883

DIGITAL-TO-ANALOG CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HDAC7542AACD/G	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7542AACD	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7542ABCD	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7542AAID/G	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7542AAID	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7542ABID	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7542AAMD/G	12-BIT DAC	CERDIP	16	MILITARY
HDAC7542AAMD	12-BIT DAC	CERDIP	16	MILITARY
HDAC7542ABMD	12-BIT DAC	CERDIP	16	MILITARY
HDAC7542A	12-BIT DAC	DIE		+25 °C

*** CONSULT FACTORY FOR AVAILABILITY**

NOTE: (X) Denotes Package Type: J - SIDEBRAZED DIP; D - CERDIP; C - LCC

ORDERING INFORMATION

DIGITAL-TO-ANALOG CONVERTERS (Continued)

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HDAC7543AACD/G	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7543AACD	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7543ABCD	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7543AAID/G	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7543AAID	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7543ABID	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7543AAMD/G	12-BIT DAC	CERDIP	16	MILITARY
HDAC7543AAMD	12-BIT DAC	CERDIP	16	MILITARY
HDAC7543ABMD	12-BIT DAC	CERDIP	16	MILITARY
HDAC7543A	12-BIT DAC	DIE		+25 °C
HDAC7545AACD/G	12-BIT DAC	CERDIP	20	COMMERCIAL
HDAC7545AACD	12-BIT DAC	CERDIP	20	COMMERCIAL
HDAC7545ABCD	12-BIT DAC	CERDIP	20	COMMERCIAL
HDAC7545AAID/G	12-BIT DAC	CERDIP	20	INDUSTRIAL
HDAC7545AAID	12-BIT DAC	CERDIP	20	INDUSTRIAL
HDAC7545ABID	12-BIT DAC	CERDIP	20	INDUSTRIAL
HDAC7545AAMD/G	12-BIT DAC	CERDIP	20	MILITARY
HDAC7545AAMD	12-BIT DAC	CERDIP	20	MILITARY
HDAC7545ABMD	12-BIT DAC	CERDIP	20	MILITARY
HDAC7545A	12-BIT DAC	DIE		+25 °C
HDAC10180AID	8-BIT, 275 MWPS DAC	CERDIP	24	INDUSTRIAL
HDAC10180BID	8-BIT, 165 MWPS DAC	CERDIP	24	INDUSTRIAL
HDAC10180AMD	8-BIT, 275 MWPS DAC	CERDIP	24	MILITARY
HDAC10180BMD	8-BIT, 165 MWPS DAC	CERDIP	24	MILITARY
HDAC10180AMD/883	8-BIT, 275 MWPS DAC	CERDIP	24	MILITARY/883
HDAC10180BMD/883	8-BIT, 165 MWPS DAC	CERDIP	24	MILITARY/883
HDAC10181AID	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC10181BID	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC10181AMD	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	MILITARY
HDAC10181BMD	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	MILITARY
HDAC10181AMD/883	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	MILITARY/883
HDAC10181BMD/883	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	MILITARY/883
HDAC51400SID	8-BIT, 400 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC51400SMD	8-BIT, 400 MWPS DAC W/REF	CERDIP	24	MILITARY
HDAC51400SMD/883	8-BIT, 400 MWPS DAC W/REF	CERDIP	24	MILITARY/883
HDAC52160AIJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	INDUSTRIAL
HDAC52160BIJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	INDUSTRIAL
HDAC52160CIJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	INDUSTRIAL
HDAC52160	16-BIT RES DAC W/REF	DIE*		+25 °C

ORDERING INFORMATION

COMPARATORS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HCMP96850SID	HIGH-SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
HCMP96850SCU	HIGH-SPEED COMPARATOR	DIE		+25 °C
HCMP96870SIC/A	DUAL HIGH-SPEED COMPARATOR	LCC	20	INDUSTRIAL
HCMP96870SID/A	DUAL HIGH-SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
HCMP96870SIJ/A	DUAL HIGH-SPEED COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
HCMP96870SIN/A	DUAL HIGH-SPEED COMPARATOR	PLASTIC DIP	16	INDUSTRIAL
HCMP96870SIP/A	DUAL HIGH-SPEED COMPARATOR	PLCC	20	INDUSTRIAL
HCMP96870	DUAL HIGH-SPEED COMPARATOR	DIE*		+25 °C
SPT9689AIJ	SUBNANOSECOND DUAL COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
SPT9689BIJ	SUBNANOSECOND DUAL COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
SPT9689AIC	SUBNANOSECOND DUAL COMPARATOR	LCC	20	INDUSTRIAL
SPT9689BIC	SUBNANOSECOND DUAL COMPARATOR	LCC	20	INDUSTRIAL
SPT9689	SUBNANOSECOND DUAL COMPARATOR	DIE*	16	+25 °C

DC/DC CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT11806M	9.3 TO 32 V OUTPUTS	MFP-8	8	-20 TO +75 °C
SPT11806Z	9.3 TO 32 V OUTPUTS	ZP-10	10	-20 TO +75 °C
SPT11821M	10 TO 24 V OUTPUTS	MFP-8	8	-20 TO +75 °C
SPT11821Z	10 TO 24 V OUTPUTS	ZP-10	10	-20 TO +75 °C

FILTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HSCF24040ACJ	LOW PASS PROGRAMMABLE FILTER	SIDEBRAZED	32	COMMERCIAL
HSCF24040ACC	LOW PASS PROGRAMMABLE FILTER	LCC*	28	COMMERCIAL
HSCF24040AMJ	LOW PASS PROGRAMMABLE FILTER	SIDEBRAZED*	32	MILITARY
HSCF24040	LOW PASS PROGRAMMABLE FILTER	DIE		+25 °C

VOLTAGE REGULATORS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT11420M	2.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11425M	2.5 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11430M	3.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11432M	3.2 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11435M	3.5 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11440M	4.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11445M	4.5 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11450M	5.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11455M	5.5 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11460M	6.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11480M	8.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT114xxMTR**	TAPE AND REEL (RIGHT)	SOT23L	6	COMMERCIAL
SPT114xxMTL**	TAPE AND REEL (LEFT)	SOT23L	6	COMMERCIAL

**** CONSULT FACTORY FOR AVAILABILITY***
***** DESIGNATOR xx DENOTES AVAILABILITY OF ANY STANDARD VOLTAGE OPTION.***

ORDERING INFORMATION

VOLTAGE REGULATORS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT11525M	2.5 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11530M	3.0 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11532M	3.2 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11535M	3.5 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11540M	4.0 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11545M	4.5 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11547M	4.7 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11550M	5.0 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11555M	5.5 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11580M	8.0 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT115xxMT**	TAPE AND REEL	MFP-8	8	COMMERCIAL
SPT11620N	2.0 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11625N	2.5 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11630N	3.0 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11635N	3.5 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11640N	4.0 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11645N	4.5 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11650N	5.0 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11655N	5.5 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT116xxNT**	PLASTIC TAPE	TO-92NT	3	COMMERCIAL

EVALUATION BOARDS

EB100A	HADC77100AIJ DEMONSTRATION BOARD
EB100B	HADC77100BIJ DEMONSTRATION BOARD
EB101A	HADC77200AIJ DEMONSTRATION BOARD
EB101B	HADC77200BIJ DEMONSTRATION BOARD
EB102B	BUFFER BOARD
EB103	HADC77200 PING-PONG BOARD
EB104	HADC574Z/674Z DEMONSTRATION BOARD
EB105	HSCF24040 DEMONSTRATION BOARD
EB7810/14	SPT7810/14 DEMONSTRATION BOARD
EB7820/24	SPT7820/24 DEMONSTRATION BOARD
EB7910/12	SPT7910/12 DEMONSTRATION BOARD
EB7920/22	SPT7920/22 DEMONSTRATION BOARD

***** DESIGNATOR xx DENOTES AVAILABILITY OF ANY STANDARD VOLTAGE OPTION.***

SIGNAL PROCESSING TECHNOLOGIES

HADC574Z

FAST, COMPLETE 12-BIT μP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

3

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI574A and AD574A
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 25 μs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit μP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The HADC574Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI574A and AD574A. Included on chip is an internal reference, clock, and a sample and hold. The S/H is an additional feature not available on similar devices.

The HADC574Z features 25 μs (Max) conversion time of 10 or 20 Volt input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit μP bus.

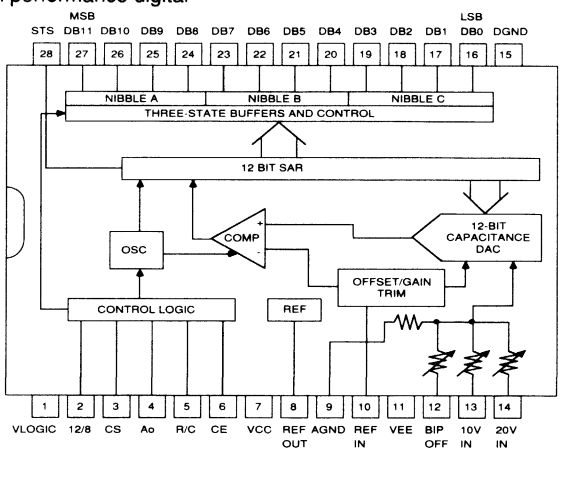
The HADC574Z is manufactured on a Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC574Z has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages
Positive Supply Voltage (V_{CC} to DGND) .... 0 to +16.5 V
Logic Supply Voltage (V_{LOGIC} to DGND) .... 0 to +7 V
Analog to Digital Ground (AGND to DGND) . -0.5 to +1 V

Input Voltages
Control Input Voltages (to DGND)
(CE, CS, Ao, 12/8, R/C) .... -0.5 to V_{LOGIC} +0.5 V
Analog Input Voltage (to AGND)
(REF IN, BIP OFF, 10 Vin) .... ±16.5 V
20 V Vin Input Voltage (to AGND) .... ±24 V

Output
Reference Output Voltage .... Indefinite short to GND
Momentary short to V_{CC}

Temperature
Operating Temperature, ambient .... -55 to +125 °C
junction .... +175 °C
Lead Temperature, (soldering 10 seconds) .... +300 °C
Storage Temperature .... -65 to +150 °C
Power Dissipation .... 1000 mW
Thermal Resistance (θ_{jA}) .... 48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		I			12			12			12	BITS
Linearity Error[1]	T_A=0 to 70 °C	I			±1			±1/2			±1/2	LSB
	T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB
	T_A = -55 to +125 °C	I			±1			±1			±1	LSB
Differential Linearity	No Missing Codes	I	11			12			12			BITS
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	I		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V,±10 V	+25 °C Adjustable to Zero	I			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	I			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
	T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS
	T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS
	With Adjustment at +25 °C											
	T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS
	T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS
	T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	TYP	MAX	HADC574ZB MIN	TYP	MAX	HADC574ZA MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4			±2			±1	LSB
					(10)			(5)			(2.5)	(ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9			±5			±2	LSB
					(45)			(25)			(10)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±12			±7			±3	LSB
					(50)			(25)			(12)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±20			±10			±5	LSB
					(50)			(25)			(12.5)	(ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		I		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		I		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		I	-5		+5	-5		+5	-5		+5	Volts
			-10		+10	-10		+10	-10		+10	Volts
Unipolar		I	0		+10	0		+10	0		+10	Volts
			0		+20	0		+20	0		+20	Volts
Input Impedance												
10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not Required for circuit operation.											
Operating Current												
I_{LOGIC}		I		0.5	1		0.5	1		0.5	1	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation +15 V, +5 V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.97	10	10.03	9.97	10	10.03	9.97	10	10.03	Volts
Output Current[4]		I			2			2			2	mA

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
DIGITAL CHARACTERISTICS												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "0"		I	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	Volts
Logic "1"		I	2.0		5.5	2.0		5.5	2.0		5.5	Volts
Current	0 to 5.5 V Input	I		±.01	+1		±.01	+1		±.01	+1	μA
Capacitance		V		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6 mA)	I			+0.4			+0.4			+0.4	Volts
Logic "1"	(I_{SOURCE} = 500 μA)	I	+2.4			+2.4			+2.4			Volts
Leakage	(High Z State, DB11-DB0 Only)	I	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	μA
Capacitance		V		5			5			5		pF

Note 1: For military temperature range, the device linearity is guaranteed to be 1/2 LSB at 25 °C.
Note 2: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.
Note 3: Full Tempco testing is performed on all Grade A and MIL-STD-883 devices.
Note 4: Available for external loads, external load should not change during conversion. When supplying an external load and operating on a +12.0 V supply, a buffer amplifier must be provided for the reference output.

ELECTRICAL SPECIFICATIONS

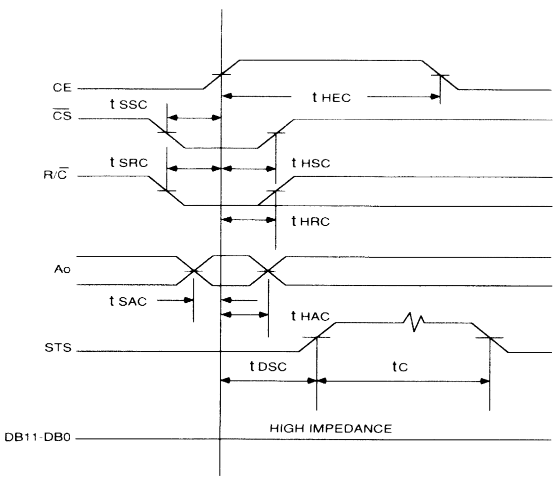
CONVERT MODE TIMING CHARACTERISTICS

T_A = +25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time												
12-Bit Cycle	T_{MIN} to T_{MAX}	I	13	18	25	15	18	25	15	18	25	µs
8-Bit Cycle	T_{MIN} to T_{MAX}	I	10	13	19	10	13	17	10	13	17	µs

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 1 - Convert Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

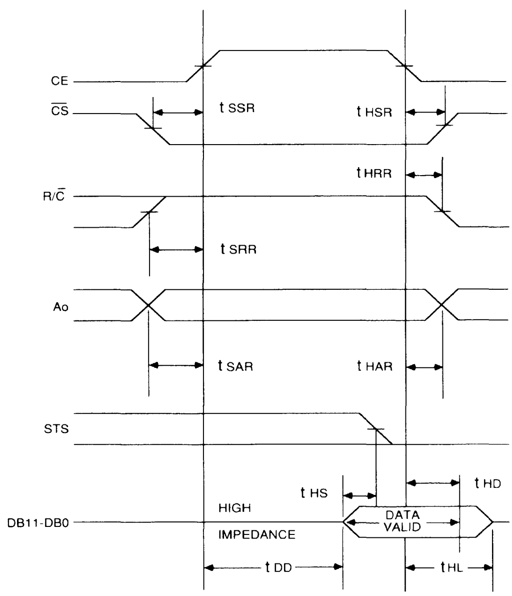
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC			HADC574ZB			HADC574ZA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (NOTE 5)												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD												
Acquisition Time		IV	1.8	2.4	3.4	1.8	2.4	3.4	1.8	2.4	3.4	µs
Aperture Uncertainty Time		V		8			8			8		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

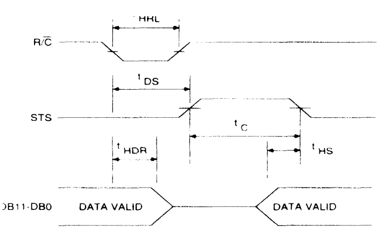
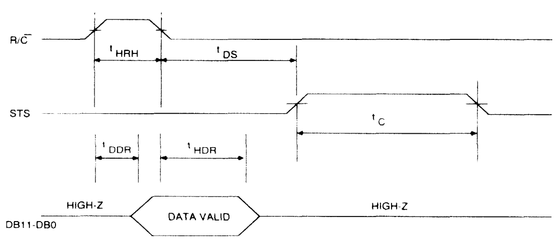


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_{JUNC} = T_{CASE} = T_{AMBIENT}$

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A= +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 6). The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 Volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC574ZAC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC574ZAM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC574Z type BC, AC, BM and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC574Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC574Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

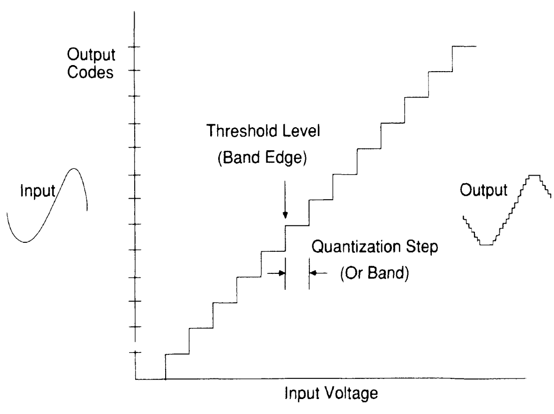
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q=FSR/2^N$ where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors (See figures 5, 6 and 7).

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

Figure 6 - Dynamic Conditions

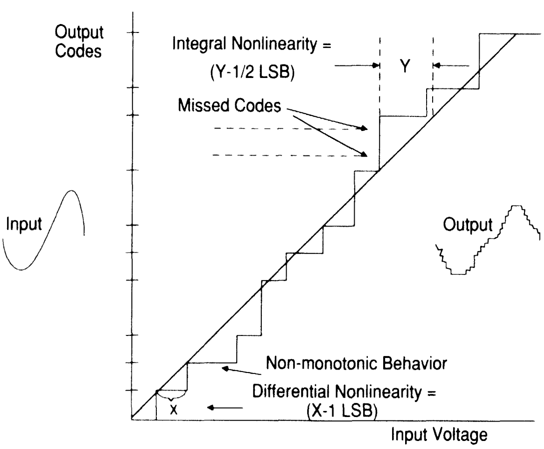
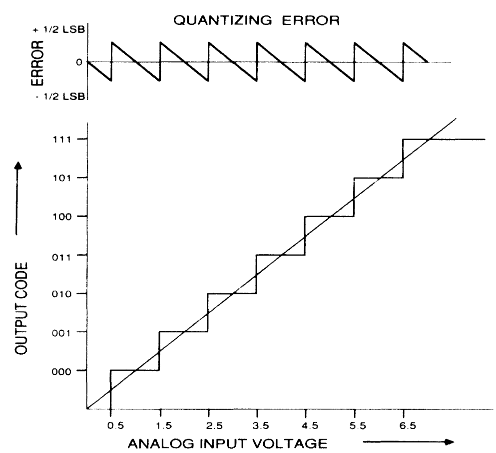


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC574Z, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

A N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature co-efficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature co-efficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC574Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in Figure 11 and 12 on page 17. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the HADC574Z assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44 mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC574Z is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The HADC574Z is a complete 12-bit analog-to-digital converter which consists of a single chip version of the industry standard 574. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample and hold, clock, output buffers and control circuitry to make possible to use the HADC574Z with few external components.

When the control section of the HADC574Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC574Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; it the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the HADC574Z is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the HADC574Z reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample and hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC574Z appear to have a built in sample and hold. This sample and hold action substantially increases the signal bandwidth of the HADC574Z over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC574Z is disconnected from the user's sample and hold. This prevents transients occurring during conversion from being inflicted upon the attached sample and hold buffer. All other 574 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

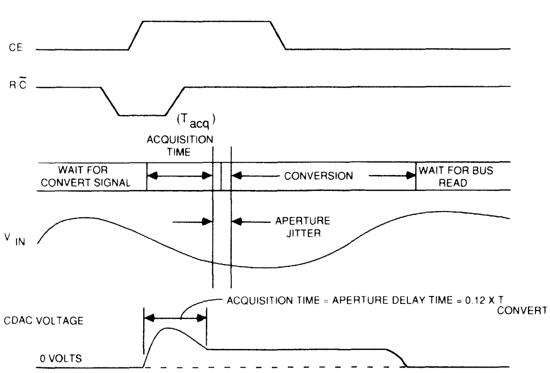
Furthermore, the isolation of the input after the acquisition time in the HADC574Z allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC574Z acts as any other 574 device because the internal S/H is transparent. The sample/hold function in the HADC574Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

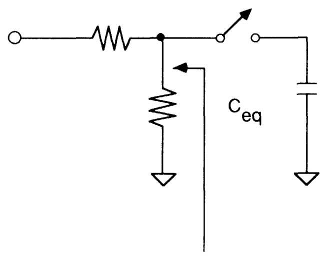
The operation of the S/H function is internal to the HADC574Z and is controlled through the normal R/$\overline{C}$ control line (refer to Figure 8). When the R/$\overline{C}$ line makes a negative transition, the HADC574Z starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

Figure 8 - Sample and Hold Function



During T_{acq}, the equivalent circuit of the HADC574Z input is as shown in Figure 9 (the time constant of the input is independent of which input level is used). This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent HADC574Z Input Circuit



R_{eq} = 4K ohms at any range

$\tau = R_{eq} C_{eq} = 100$ nsec.

Note that because the sample is taken relative to the R/$\overline{C}$ transition, Tacq is also the traditional "aperture delay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} =2.4 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HADC574Z.

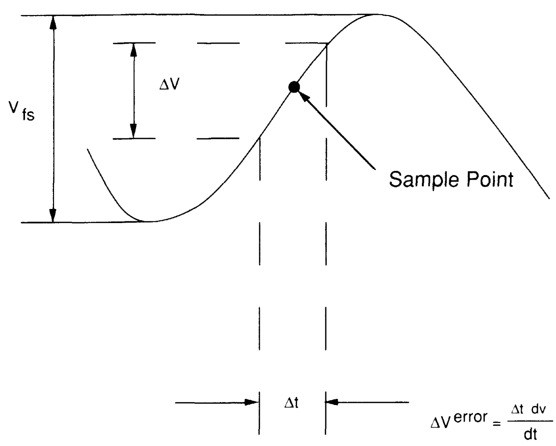
APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time that the actual sample is taken i.e. the "aperture jitter' or T_{AJ}. The HADC574Z has a nominal aperture jitter of 8 nsecs between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (see Figure 10). The magnitude of this change for a sine wave can be calculated:

$Verr \leq V_{fs}/2^{N+1}$ (where Verr is the allowable error voltage and Vfs is the full scale voltage)

Figure 10 - Aperture Uncertainty



From Figure 10:

$Sr = \Delta V/\Delta T = 2\ \pi f Vp$

Let $\Delta V = Verr = V_{fs} 2^{-(N+1)}$, $Vp = Vin/2$ and $\Delta T = t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{fs}/2^{N+1} \geq \pi f Vin\ t_{AJ}$ or $f_{max} \leq V_{fs}/(\pi Vin\ t_{AJ}) 2N+1$

For the HADC574Z, T_{AJ}=8 nsec, therefore $f_{max} \leq$5 kHz.

For higher frequency signal inputs, an external sample and hold is recommended.

TYPICAL INTERFACE CIRCUIT

The HADC574Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figure 11 and 12. The two typical interface circuits are for operating the HADC574Z in either an unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few conditions concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as close to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC574Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being pickup by the converter.

Capacitor bypass pairs are needed from each supply pin to it's respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC574Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC574Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

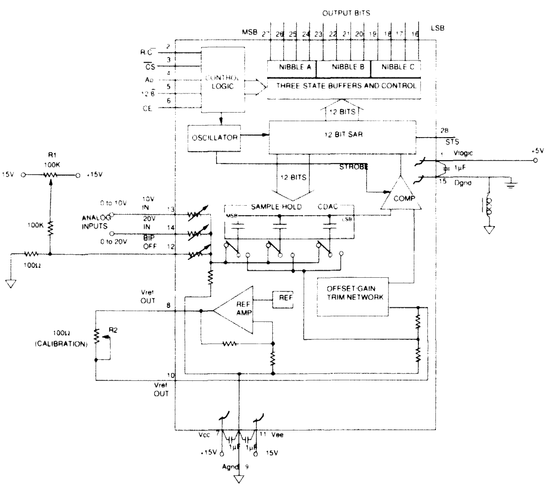
UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the HADC574Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

Figure 11 - Unipolar Input Connections



BIPOLAR

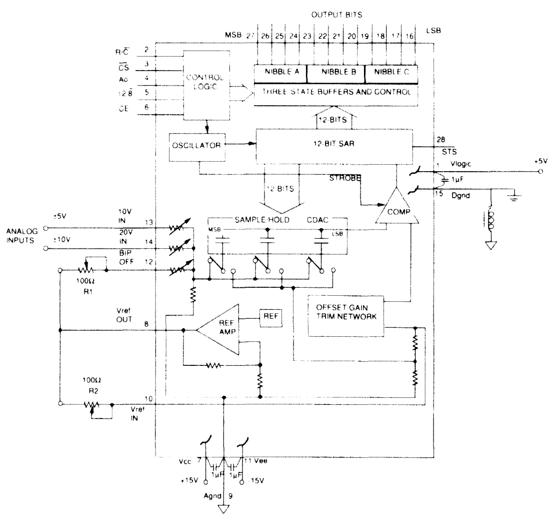
The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 by 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 by 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 12 - Bipolar Input Connections



CONTROLLING THE HADC574Z

The HADC574Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 following by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operations is shown in Table I, and the internal control logic is shown in a simplified schematic in Figure 14.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The other controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in Figures 3 and 4. It may have a duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Figure 13 - Interfacing the HADC574Z to an 8-bit Data Bus

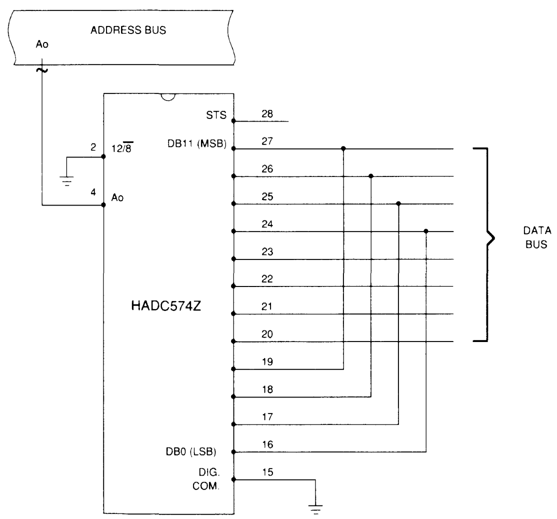


Table I - Truth Table for the HADC574Z Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table I. The latched state determines if the conversion stops with 8-bit (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in Table I. The last of the three to reach the correct state starts the conversions, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50 ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new start of Ao and possible cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high, and $\overline{CS}$ is low. That data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:

BYTE 1

XXXX XXXX

MSB

BYTE 2

XXXX 0000

LSB

This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the address bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is completed and STS is low. If earlier access is needed, the read can begin no later than the addition of time t_{DD} and t_{HS} before STS goes low.

Figure 14 - Control Logic

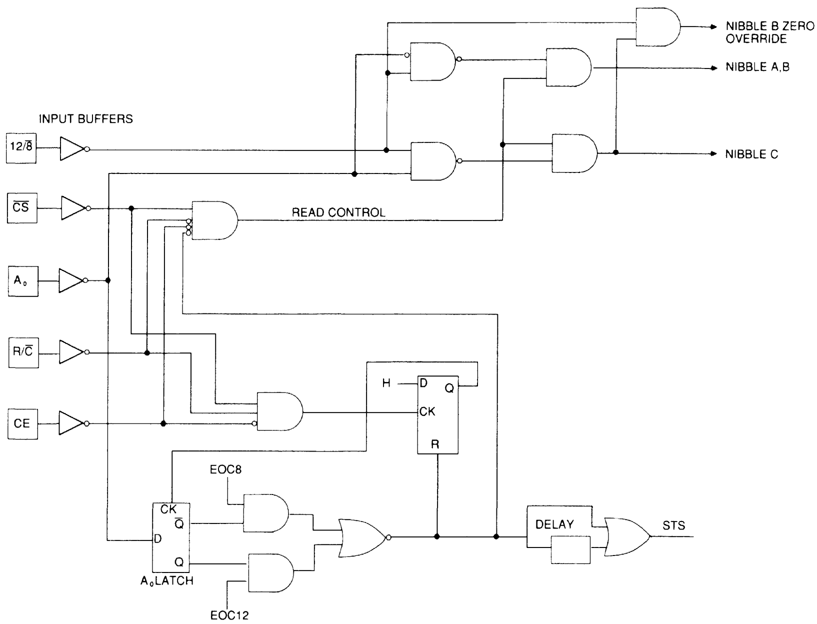
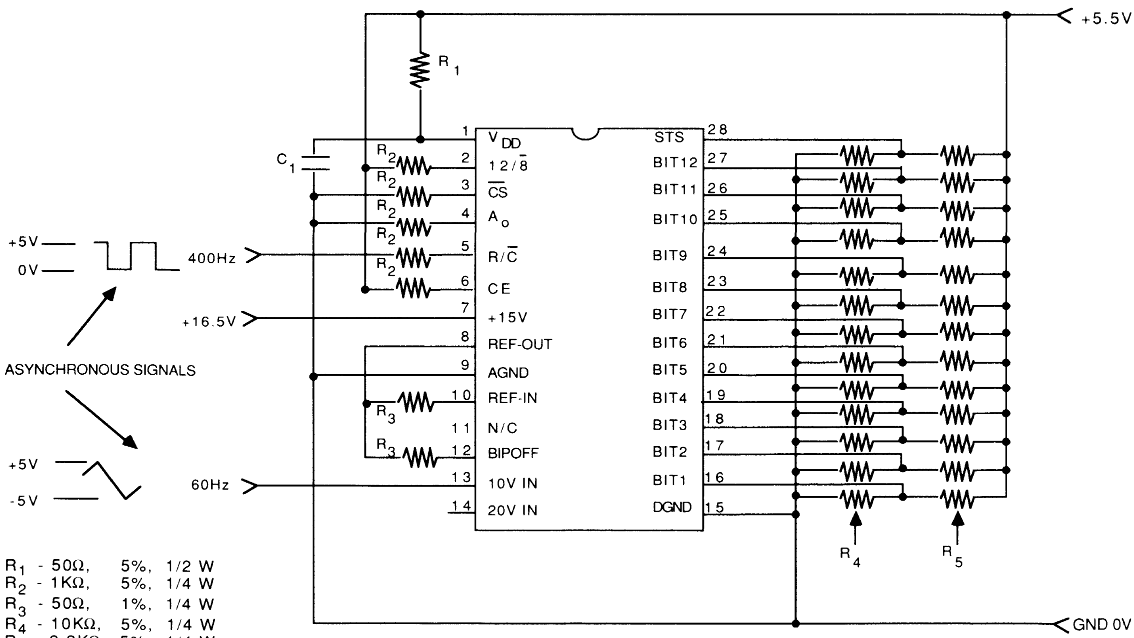
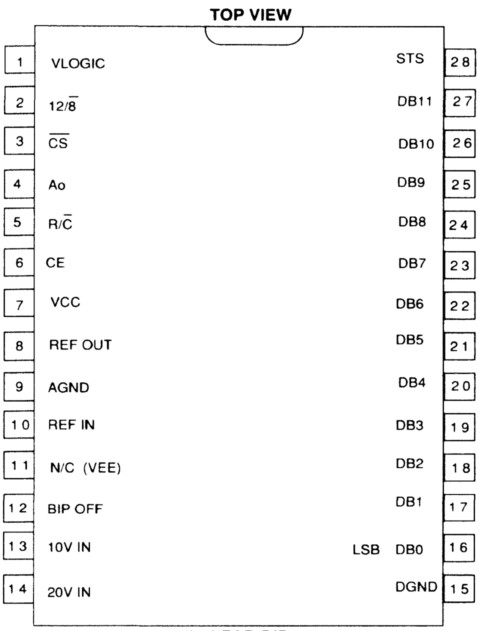


Figure 15 - Burn-In Schematic

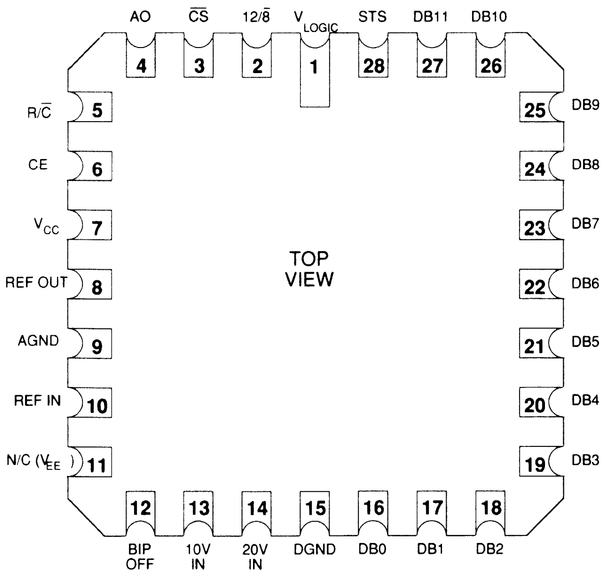


R1 - 50Ω, 5%, 1/2 W
R2 - 1KΩ, 5%, 1/4 W
R3 - 50Ω, 1%, 1/4 W
R4 - 10KΩ, 5%, 1/4 W
R5 - 3.3KΩ, 5%, 1/4 W
C1 - 1µF, 5%

PIN Assignment HADC574Z



28 LEAD DIP



PIN Functions HADC574Z

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5 V
12/$\overline{8}$	Data Mode Selection
$\overline{CS}$	Chip Selection
Ao	Byte Address/Short Cycle
R/$\overline{C}$	Read/Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage, Nominally +15 V
REF OUT	Reference Output, Nominally +10 V
AGND*	Analog Ground
REF IN	Reference Input
N/C (V_{EE})	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10 V IN	10 Volt Analog Input
20 V IN	20 Volt Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

* The lid on the sidebrazed and LCC packages are internally connected to AGND.

SPT

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

HADC674Z

FAST, COMPLETE 12-BIT µP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI674A
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 15 µs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit µP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

3

GENERAL DESCRIPTION

The HADC674Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI674A. Included on chip is an internal reference, clock, and a sample and hold. The S/H is an additional feature not available on similar devices.

The HADC674Z features 15 µs (Max) conversion time of 10 or 20 Volt input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit µP bus.

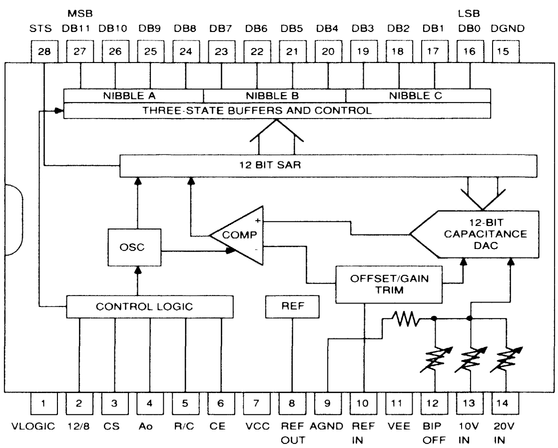
The HADC674Z is manufactured on a Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC674Z has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages
- Positive Supply Voltage (V_{CC} to DGND) .... 0 to +16.5 V
- Logic Supply Voltage (V_{LOGIC} to DGND) .... 0 to +7 V
- Analog to Digital Ground (AGND to DGND) . -0.5 to +1 V

Input Voltages
- Control Input Voltages (to DGND)
- (CE, CS, Ao, 12/8, R/C) .... -0.5 to V_{LOGIC} +0.5 V
- Analog Input Voltage (to AGND)
- (REF IN, BIP OFF, 10 Vin) .... ±16.5 V
- 20 V Vin Input Voltage (to AGND) .... ±24 V

Output
- Reference Output Voltage .... Indefinite short to GND
- Momentary short to V_{CC}

Temperature
- Operating Temperature, ambient .... -55 to +125 °C
- junction .... +175 °C
- Lead Temperature, (soldering 10 seconds) .... +300 °C
- Storage Temperature .... -65 to +150 °C
- Power Dissipation .... 1000 mW
- Thermal Resistance (θ_{jA}) .... 48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		I			12			12			12	BITS
Linearity Error[1]	T_A=0 to 70 °C	I			±1			±1/2			±1/2	LSB
	T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB
	T_A = -55 to +125 °C	I			±1			±1			±1	LSB
Differential Linearity	No Missing Codes	I	11			12			12			BITS
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	I		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V,±10 V	+25 °C Adjustable to Zero	I			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	I			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
	T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS
	T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS
	With Adjustment at +25 °C											
	T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS
	T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS
	T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)
	T_A = -25 to +85 °C	IV			±12 (50)			±7 (25)			±3 (12)	LSB (ppm/°C)
	T_A = -55 to +125 °C	IV			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		I		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		I		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		I	-5 -10		+5 +10	-5 -10		+5 +10	-5 -10		+5 +10	Volts Volts
Unipolar		I	0 0		+10 +20	0 0		+10 +20	0 0		+10 +20	Volts Volts
Input Impedance 10 Volt Span 20 Volt Span		I	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 kΩ kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not Required for circuit operation.											
Operating Current												
I_{LOGIC}		I		0.5	1		0.5	1		0.5	1	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation +15 V, +5 V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.97	10	10.03	9.97	10	10.03	9.97	10	10.03	Volts
Output Current[4]		I			2			2			2	mA

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DIGITAL CHARACTERISTICS												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "0"		I	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	Volts
Logic "1"		I	2.0		5.5	2.0		5.5	2.0		5.5	Volts
Current	0 to 5.5 V Input	I		±.01	+1		±.01	+1		±.01	+1	µA
Capacitance		V		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6 mA)	I			+0.4			+0.4			+0.4	Volts
Logic "1"	(I_{SOURCE} = 500 µA)	I	+2.4			+2.4			+2.4			Volts
Leakage	(High Z State, DB11-DB0 Only)	I	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		V		5			5			5		pF

Note 1: For military temperature range, the device linearity is guaranteed to be 1/2 LSB at 25 °C.
Note 2: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.
Note 3: Full Tempco testing is performed on all Grade A and MIL-STD-883 devices.
Note 4: Available for external loads, external load should not change during conversion. When supplying an external load and operating on a +12.0 V supply, a buffer amplifier must be provided for the reference output.

ELECTRICAL SPECIFICATIONS

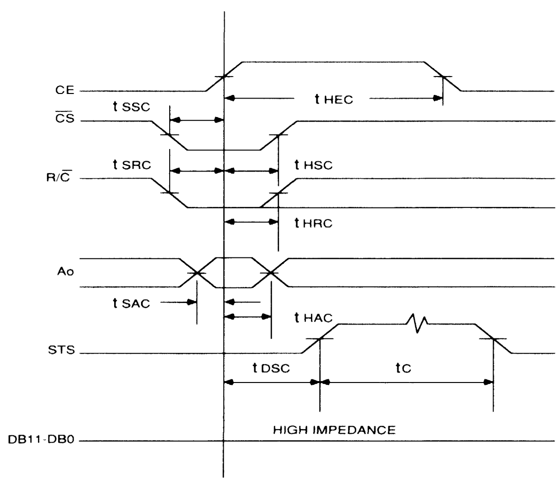
CONVERT MODE TIMING CHARACTERISTICS

T_A = +25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time												
12-Bit Cycle	T_{MIN} to T_{MAX}	I	9	13	15	9	13	15	9	13	15	µs
8-Bit Cycle	T_{MIN} to T_{MAX}	I	6	8	10	6	8	10	6	8	10	µs

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 1 - Convert Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

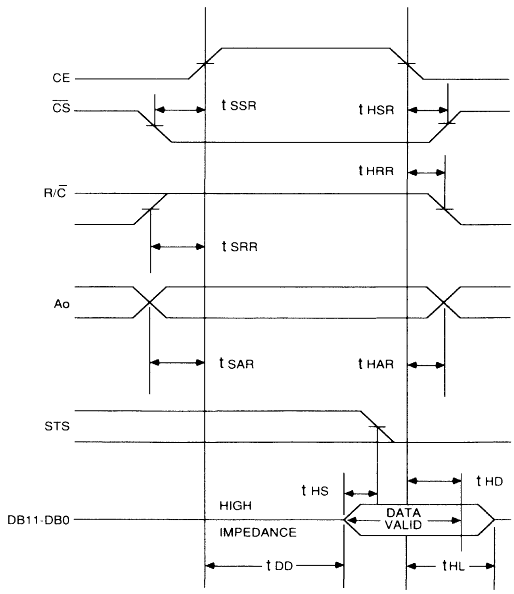
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (NOTE 5)												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD												
Acquisition Time		IV	1.2	1.7	2.0	1.2	1.7	2.0	1.2	1.7	2.0	µs
Aperture Uncertainty Time		V		8			8			8		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

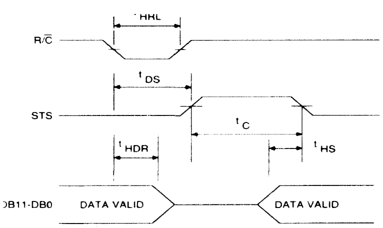
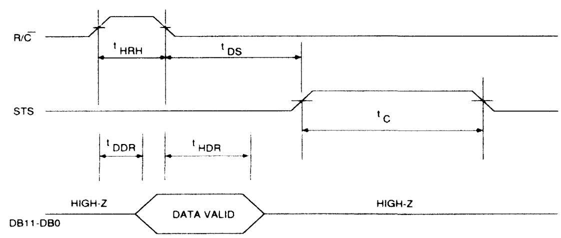


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_{JUNC} = T_{CASE} = T_{AMBIENT}$

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A= +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 6). The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 Volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC674ZAC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC674ZAM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC674Z type BC, AC, BM and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC674Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC674Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

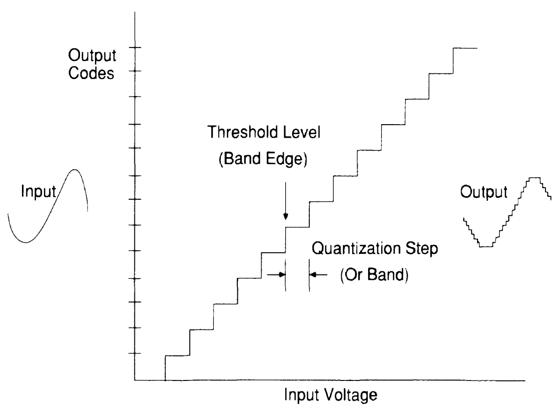
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q=FSR/2^N where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors (See figures 5, 6 and 7).

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

Figure 6 - Dynamic Conditions

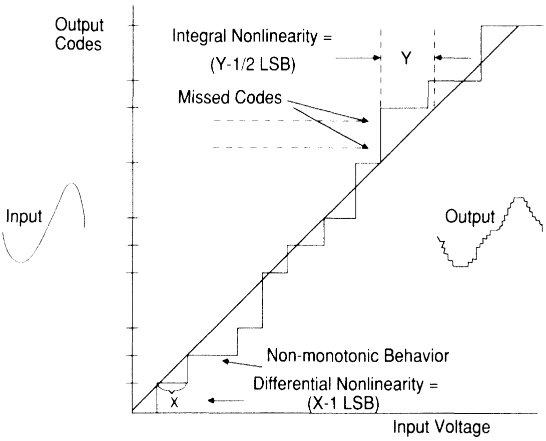
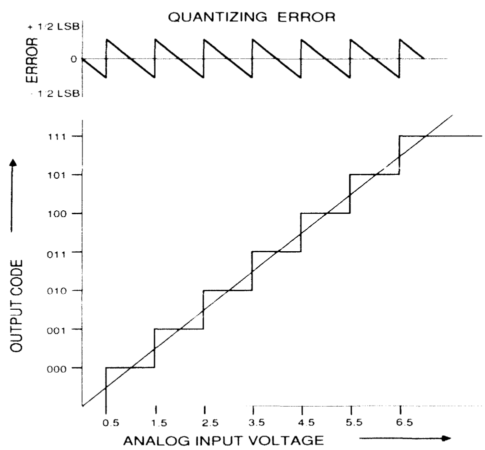


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC674Z, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

A N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature co-efficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature co-efficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC674Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in Figure 11 and 12 on page 17. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the HADC674Z assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44 mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC674Z is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The HADC674Z is a complete 12-bit analog-to-digital converter which consists of a single chip version of the industry standard 674. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample and hold, clock, output buffers and control circuitry to make possible to use the HADC674Z with few external components.

When the control section of the HADC674Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or restarted and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC674Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; it the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the HADC674Z is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the HADC674Z reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample and hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC674Z appear to have a built in sample and hold. This sample and hold action substantially increases the signal bandwidth of the HADC674Z over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC674Z is disconnected from the user's sample and hold. This prevents transients occurring during conversion from being inflicted upon the attached sample and hold buffer. All other 674 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

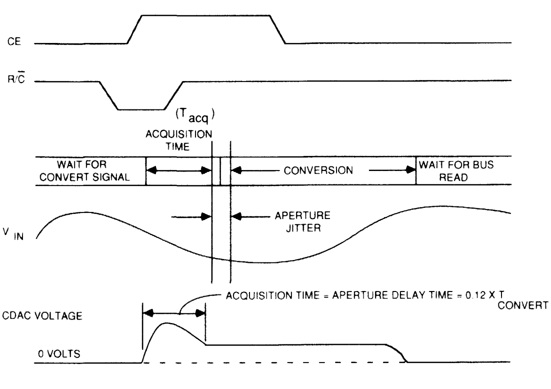
Furthermore, the isolation of the input after the acquisition time in the HADC674Z allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC674Z acts as any other 674 device because the internal S/H is transparent. The sample/hold function in the HADC674Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

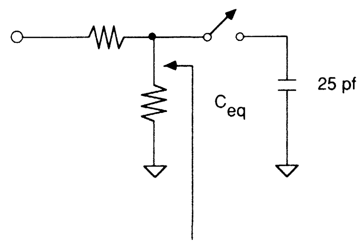
The operation of the S/H function is internal to the HADC674Z and is controlled through the normal R/$\overline{C}$ control line (refer to Figure 8). When the R/$\overline{C}$ line makes a negative transition, the HADC674Z starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

Figure 8 - Sample and Hold Function



During T_{acq}, the equivalent circuit of the HADC674Z input is as shown in Figure 9 (the time constant of the input is independent of which input level is used). This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent HADC674Z Input Circuit



R_{eq} = 4K ohms at any range

$\tau = R_{eq} C_{eq} = 100$ nsec.

Note that because the sample is taken relative to the R/$\overline{C}$ transition, Tacq is also the traditional "aperturedelay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} =1.7 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HADC674Z.

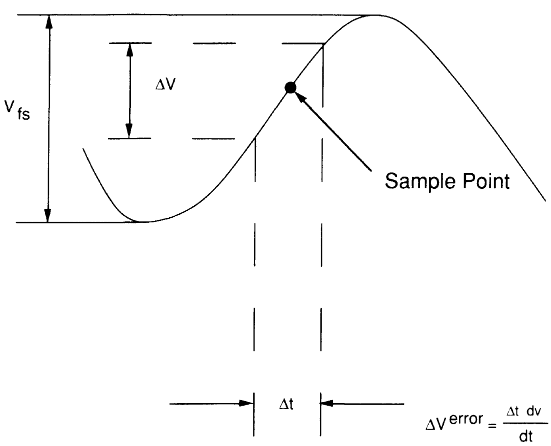
APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time that the actual sample is taken, i.e., the "aperture jitter" or T_{AJ}. The HADC674Z has a nominal aperture jitter of 8 nsecs between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (see Figure 10). The magnitude of this change for a sine wave can be calculated:

$Verr \leq V_{fs}/2^{N+1}$ (where Verr is the allowable error voltage and Vfs is the full scale voltage)

Figure 10 - Aperture Uncertainty



From Figure 10:

$Sr=\Delta V/\Delta T=2\ \pi fVp$

Let $\Delta V=Verr=V_{fs}2^{-(N+1)}$, $Vp=Vin/2$ and $\Delta T=t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{fs}/2^{N+1}\geq \pi fVin\ t_{AJ}$ or $f_{max} \leq V_{fs}/(\pi Vin\ t_{AJ})2N+1$

For the HADC674Z, T_{AJ}=8 nsec, therefore f_{max} ≤5 kHz.

For higher frequency signal inputs, an external sample and hold is recommended.

TYPICAL INTERFACE CIRCUIT

The HADC674Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figure 11 and 12. The two typical interface circuits are for operating the HADC674Z in either an unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few conditions concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as close to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC674Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being pickup by the converter.

Capacitor bypass pairs are needed from each supply pin to it's respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC674Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC674Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

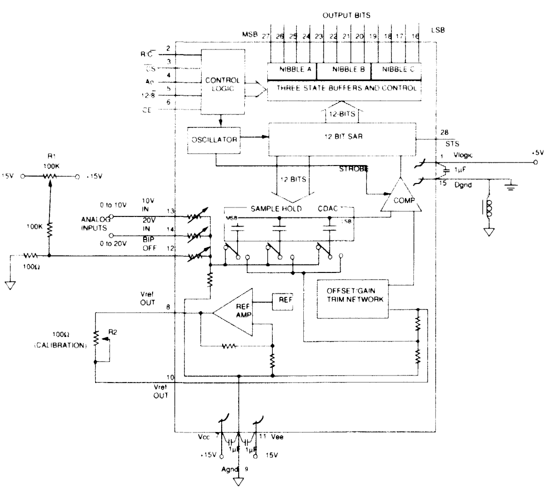
UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the HADC674Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

Figure 11 - Unipolar Input Connections



BIPOLAR

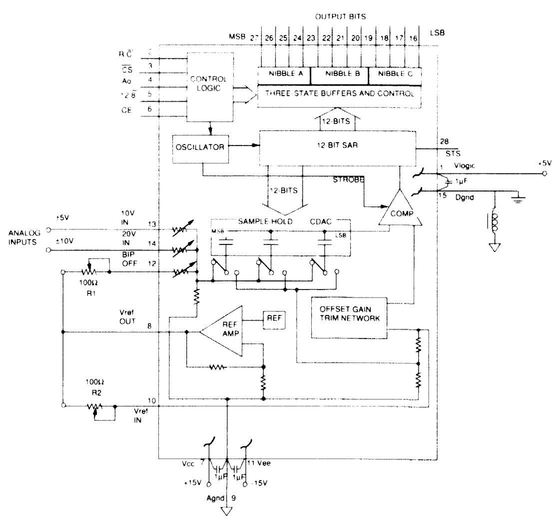
The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 by 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 by 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 12 - Bipolar Input Connections



CONTROLLING THE HADC674Z

The HADC674Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 following by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operations is shown in Table I, and the internal control logic is shown in a simplified schematic in Figure 14.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The other controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in Figures 3 and 4. It may have a duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Figure 13 - Interfacing the HADC674Z to an 8-bit Data Bus

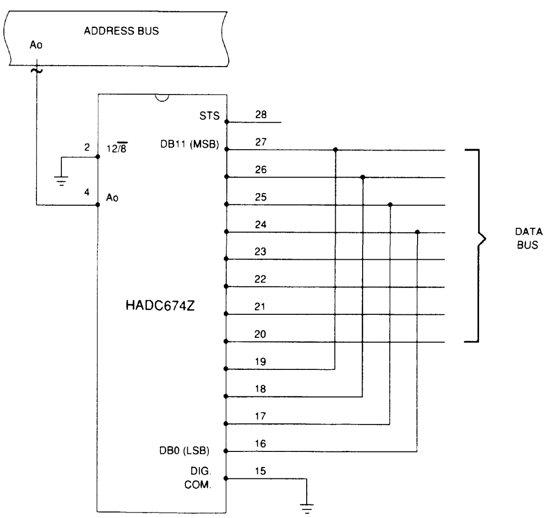


Table I - Truth Table for the HADC674Z Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table I. The latched state determines if the conversion stops with 8-bit (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in Table I. The last of the three to reach the correct state starts the conversions, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50 ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new start of Ao and possible cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high, and $\overline{CS}$ is low. That data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:

BYTE 1

XXXX XXXX

MSB

BYTE 2

XXXX 0000

LSB

This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the address bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is completed and STS is low. If earlier access is needed, the read can begin no later than the addition of time t_{DD} and t_{HS} before STS goes low.

Figure 14 - Control Logic

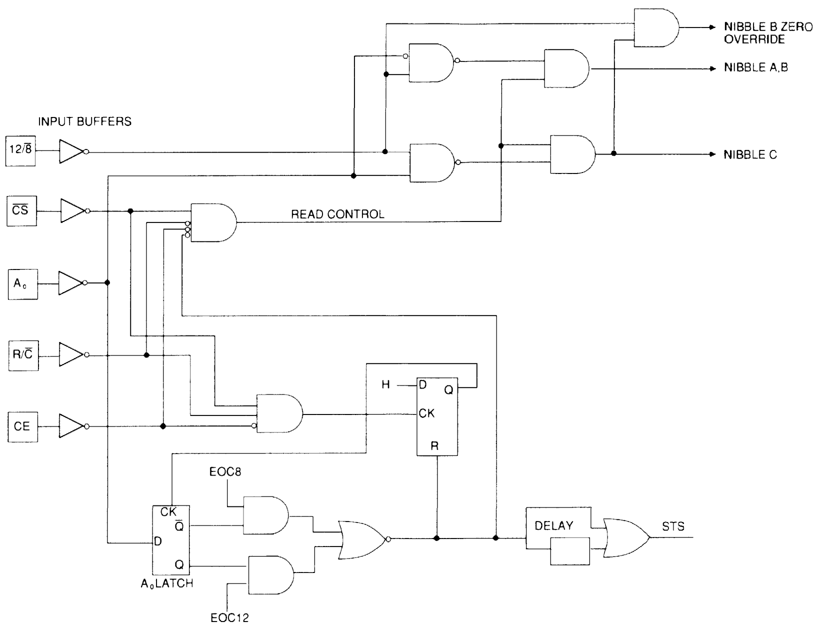
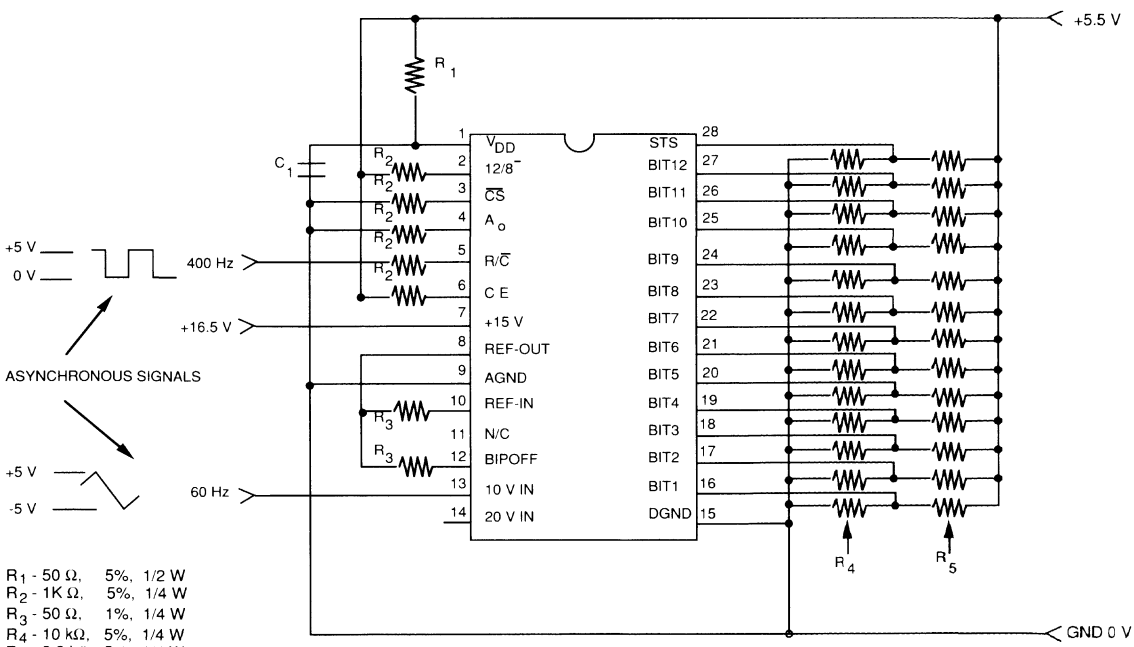
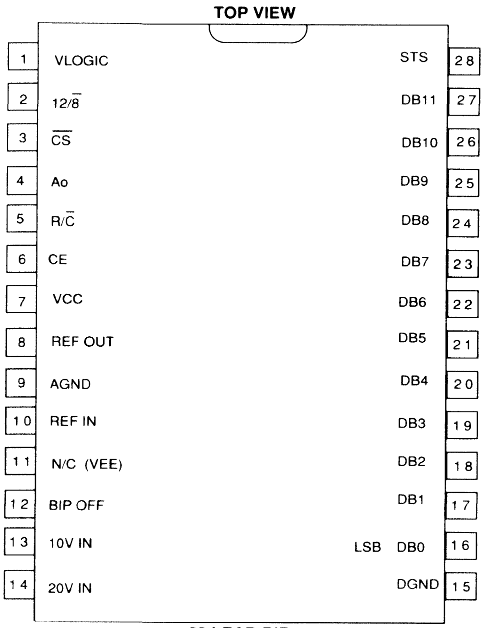


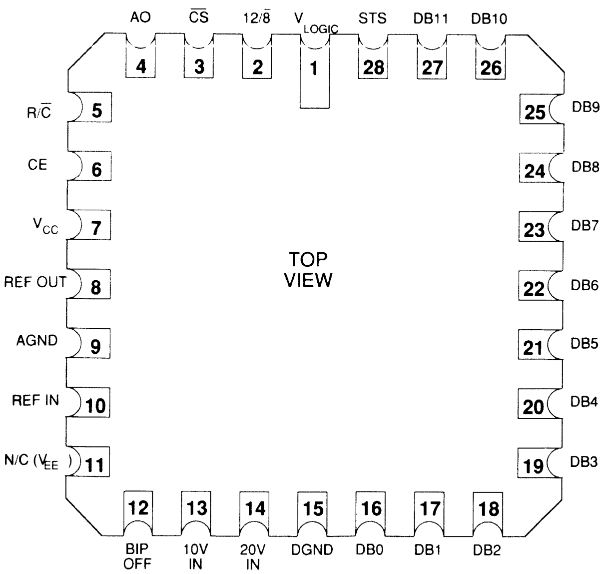
Figure 15 - Burn-In Schematic



R_1 - 50 Ω, 5%, 1/2 W
R_2 - 1K Ω, 5%, 1/4 W
R_3 - 50 Ω, 1%, 1/4 W
R_4 - 10 kΩ, 5%, 1/4 W
R_5 - 3.3 kΩ, 5%, 1/4 W
C_1 - 1 μF, 5%

PIN Assignment HADC674Z





PIN Functions HADC674Z

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5 V
12/$\overline{8}$	Data Mode Selection
$\overline{CS}$	Chip Selection
Ao	Byte Address/Short Cycle
R/$\overline{C}$	Read/Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage, Nominally +15 V
REF OUT	Reference Output, Nominally +10 V
AGND*	Analog Ground
REF IN	Reference Input
N/C (V_{EE})	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10 V IN	10 Volt Analog Input
20 V IN	20 Volt Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

* The lid on the sidebrazed and LCC packages are internally connected to AGND.

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

SPT774

FAST, COMPLETE 12-BIT μP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

ADVANCE INFORMATION

3

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI774
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 8 μs Max Conversion Time Including S/H Acquisition
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit μP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The SPT774 is a complete, 12-bit successive approximation A/D converter. Included on chip is an internal reference, clock, and a sample and hold. The S/H allows full nyquist sampling of input signals.

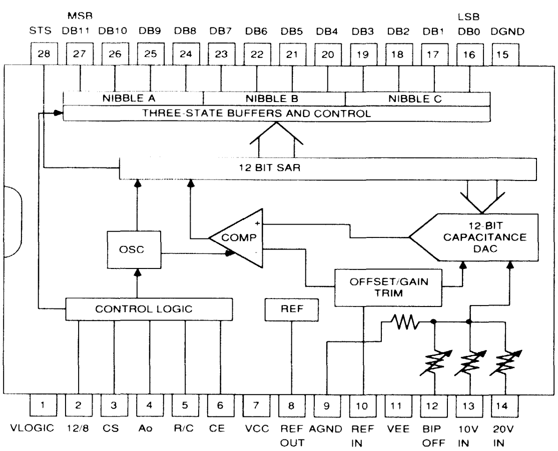
The SPT774 features 8 μs (Max) conversion time of 10 or 20 Volt input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit μP bus.

The BIMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film available on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The SPT774 has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} to DGND) .... 0 to +16.5 V
Logic Supply Voltage (V_{LOGIC} to DGND) .... 0 to +7 V
Analog to Digital Ground (AGND to DGND) . -0.5 to +1 V

Input Voltages

Control Input Voltages (to DGND)
(CE, CS, Ao, 12/8, R/C) .... -0.5 to V_{LOGIC} +0.5 V
Analog Input Voltage (to AGND)
(REF IN, BIP OFF, 10 Vin) .... ±16.5 V
20 V Vin Input Voltage (to AGND) .... ±24 V

Output

Reference Output Voltage .... Indefinite short to GND
Momentary short to V_{CC}

Temperature

Operating Temperature, ambient .... -55 to +125 °C
junction .... +175 °C
Lead Temperature, (soldering 10 seconds)........ +300 °C
Storage Temperature .... -65 to +150 °C
Power Dissipation .... 1000 mW
Thermal Resistance (θ_{jA}) .... 48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		I			12			12			12	BITS
Linearity Error[1]	T_A=0 to 70 °C	I			±1			±1/2			±1/2	LSB
	T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB
	T_A = -55 to +125 °C	I			±1			±1			±1	LSB
Differential Linearity	No Missing Codes	I	11			12			12			BITS
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	I		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V,±10 V	+25 °C Adjustable to Zero	I			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	I			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
	T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS
	T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS
	With Adjustment at +25 °C											
	T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS
	T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS
	T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)
	T_A = -25 to +85 °C	IV			±12 (50)			±7 (25)			±3 (12)	LSB (ppm/°C)
	T_A = -55 to +125 °C	IV			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		I		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		I		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		I	-5		+5	-5		+5	-5		+5	Volts
			-10		+10	-10		+10	-10		+10	Volts
Unipolar		I	0		+10	0		+10	0		+10	Volts
			0		+20	0		+20	0		+20	Volts
Input Impedance												
10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not Required for circuit operation.											
Operating Current												
I_{LOGIC}		I		0.5	1		0.5	1		0.5	1	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation +15 V, +5 V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.97	10	10.03	9.97	10	10.03	9.97	10	10.03	Volts
Output Current[4]		I			2			2			2	mA

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
DIGITAL CHARACTERISTICS												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "0"		I	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	Volts
Logic "1"		I	2.0		5.5	2.0		5.5	2.0		5.5	Volts
Current	0 to 5.5 V Input	I		±.01	+1		±.01	+1		±.01	+1	µA
Capacitance		V		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6 mA)	I			+0.4			+0.4			+0.4	Volts
Logic "1"	(I_{SOURCE} = 500 µA)	I	+2.4			+2.4			+2.4			Volts
Leakage	(High Z State, DB11-DB0 Only)	I	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		V		5			5			5		pF

Note 1: For military temperature range, the device linearity is guaranteed to be 1/2 LSB at 25 °C.
Note 2: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.
Note 3: Full Tempco testing is performed on all Grade A and MIL-STD-883 devices.
Note 4: Available for external loads, external load should not change during conversion. When supplying an external load and operating on a +12.0 V supply, a buffer amplifier must be provided for the reference output.

ELECTRICAL SPECIFICATIONS

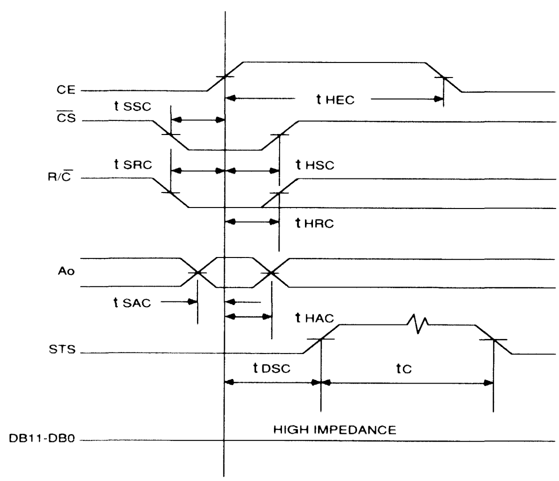
CONVERT MODE TIMING CHARACTERISTICS

T_A = +25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time												
12-Bit Cycle	T_{MIN} to T_{MAX}	I	6	7	8	6	7	8	6	7	8	µs
8-Bit Cycle	T_{MIN} to T_{MAX}	I	4.85	5.25	5.65	4.85	5.25	5.65	4.85	5.25	5.65	µs

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 1 - Convert Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

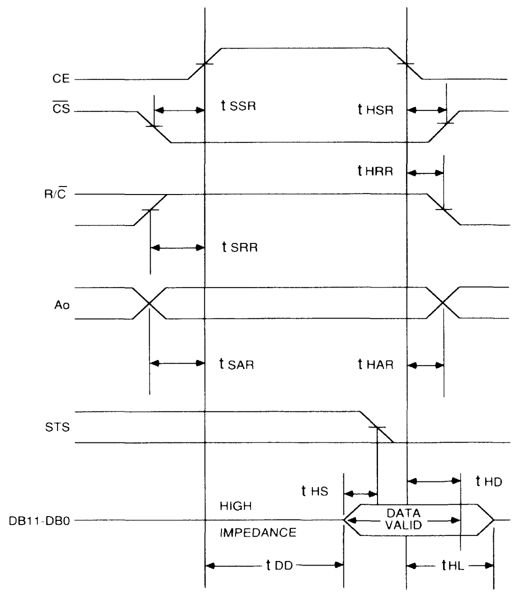
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	90		300	90		300	90		300	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
AC ELECTRICAL CHARACTERISTICS (NOTE 5)												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD												
Acquisition Time		IV	1.2	1.3	1.4	1.2	1.3	1.4	1.2	1.3	1.4	µs
Aperture Uncertainty Time		V		1			1			1		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

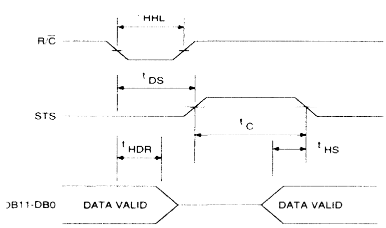
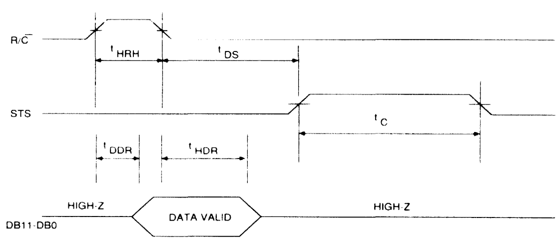


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_{JUNC} = T_{CASE} = T_{AMBIENT}$

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A= +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 6). The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 Volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The SPT774AC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The SPT774AM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the SPT774 type BC, AC, BM and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The SPT774 CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The SPT774's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

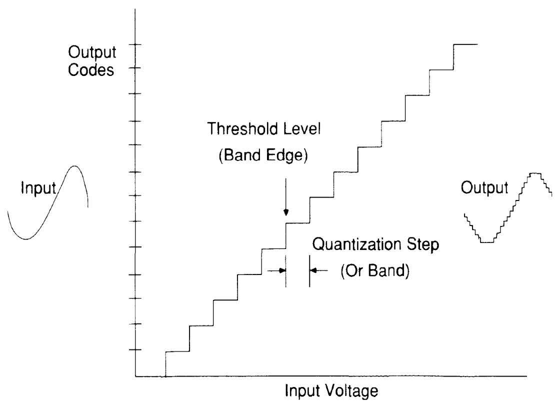
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q=FSR/2^N where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors (See figures 5, 6 and 7).

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

Figure 6 - Dynamic Conditions

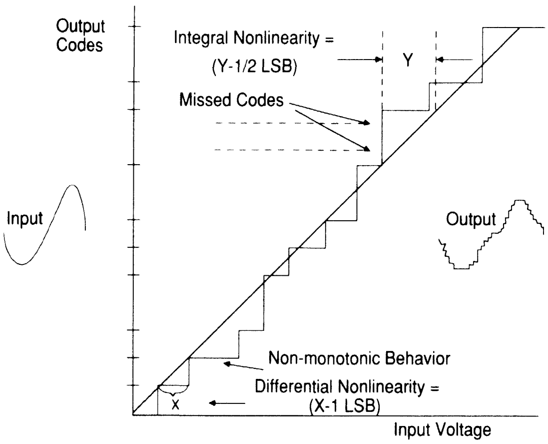
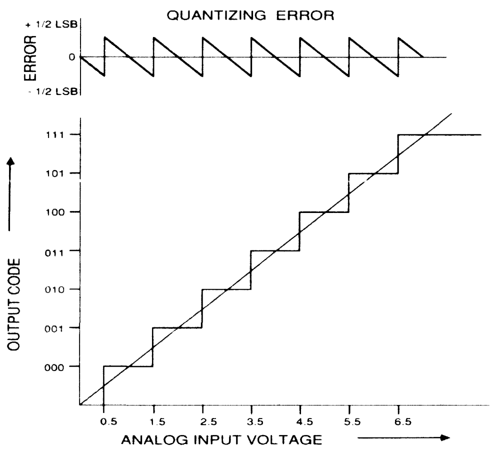


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the SPT774, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

A N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature co-efficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature co-efficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The SPT774 is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in Figure 11 and 12 on page 17. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the SPT774 assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44 mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the SPT774 is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The SPT774 is a complete 12-bit analog-to-digital converter which consists of a single chip version of the industry standard 774. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample and hold, clock, output buffers and control circuitry to make possible to use the SPT774 with few external components.

When the control section of the SPT774 initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal SPT774 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; it the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the SPT774 is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the SPT774 reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample and hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the SPT774 appear to have a built in sample and hold. This sample and hold action substantially increases the signal bandwidth of the SPT774 over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the SPT774 is disconnected from the user's sample and hold. This prevents transients occurring during conversion from being inflicted upon the attached sample and hold buffer. All other 774 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

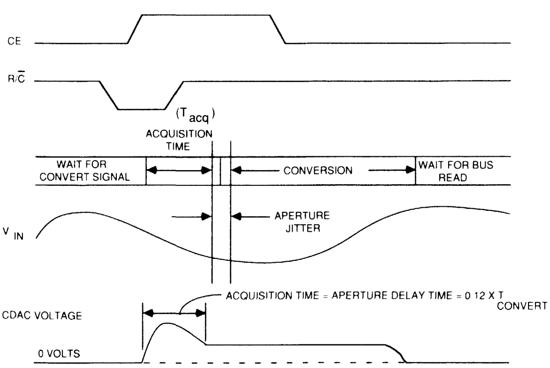
Furthermore, the isolation of the input after the acquisition time in the SPT774 allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the SPT774 acts as any other 774 device because the internal S/H is transparent. The sample/hold function in the SPT774 is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

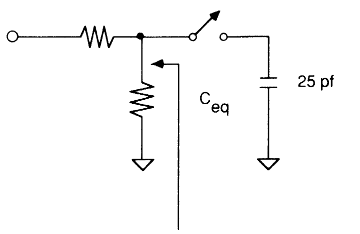
The operation of the S/H function is internal to the SPT774 and is controlled through the normal R/$\overline{C}$ control line (refer to Figure 8). When the R/$\overline{C}$ line makes a negative transition, the SPT774 starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

Figure 8 - Sample and Hold Function



During T_{acq}, the equivalent circuit of the SPT774 input is as shown in Figure 9 (the time constant of the input is independent of which input level is used). This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent SPT774 Input Circuit



R_{eq} = 4K ohms at any range

$\tau = R_{eq} C_{eq}$ = 100 nsec.

Note that because the sample is taken relative to the R/$\overline{C}$ transition, Tacq is also the traditional "aperture delay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} =1.3 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the SPT774.

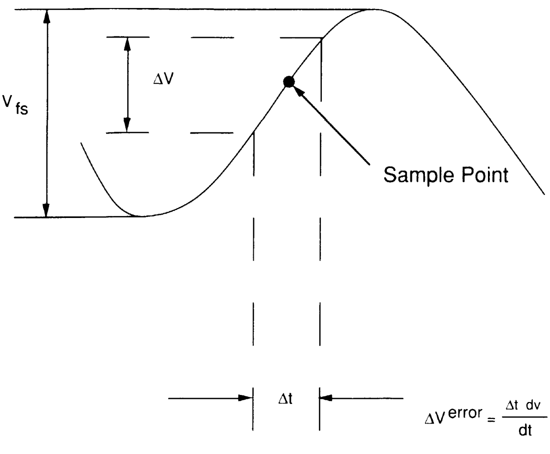
APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time that the actual sample is taken, i.e., the "aperture jitter" or T_{AJ}. The SPT774 has a nominal aperture jitter of 8 nsecs between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (see Figure 10). The magnitude of this change for a sine wave can be calculated:

$Verr \leq V_{fs}/2^{N+1}$ (where Verr is the allowable error voltageand Vfs is the full scale voltage)

Figure 10 - Aperture Uncertainty



From Figure 10:

$Sr=\Delta V/\Delta T=2\ \pi fVp$

Let $\Delta V=Verr=V_{fs}2^{-(N+1)}$, Vp=Vin/2 and $\Delta T=t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{fs}/2^{N+1}\geq\pi fVin\ t_{AJ}$ or $f_{max}\leq V_{fs}/(\pi Vin\ t_{AJ})2N+1$

For the SPT774, T_{AJ}=1 nsec, therefore $f_{max}\leq$40 kHz.

For higher frequency signal inputs, an external sample and hold is recommended.

TYPICAL INTERFACE CIRCUIT

The SPT774 is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figure 11 and 12. The two typical interface circuits are for operating the SPT774 in either an unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few conditions concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as close to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the SPT774 must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being pickup by the converter.

Capacitor bypass pairs are needed from each supply pin to it's respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the SPT774 is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The SPT774 may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

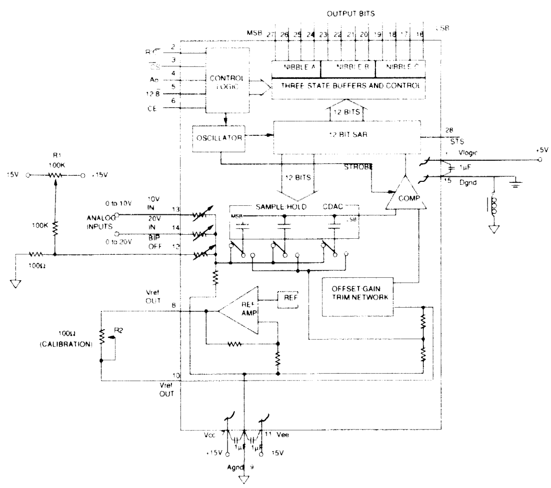
UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the SPT774. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

Figure 11 - Unipolar Input Connections



BIPOLAR

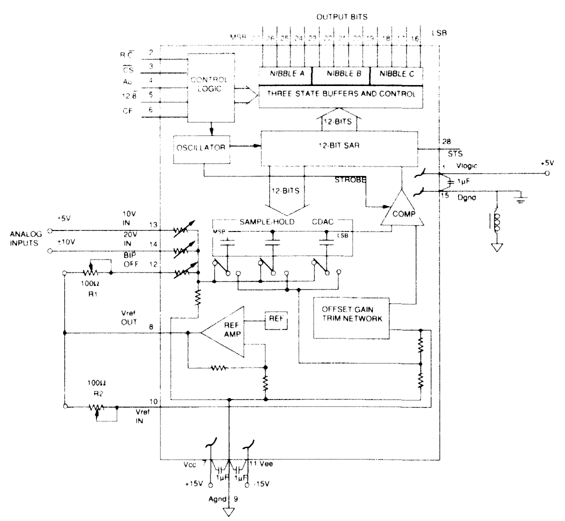
The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 by 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 by 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 12 - Bipolar Input Connections



CONTROLLING THE SPT774

The SPT774 can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 following by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operations is shown in Table I, and the internal control logic is shown in a simplified schematic in Figure 14.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The other controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in Figures 3 and 4. It may have a duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Figure 13 - Interfacing the SPT774 to an 8-bit Data Bus

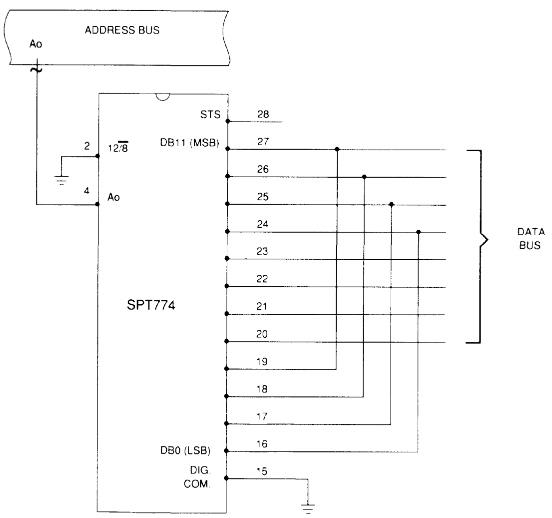


Table I - Truth Table for the SPT774 Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table I. The latched state determines if the conversion stops with 8-bit (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in Table I. The last of the three to reach the correct state starts the conversions, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50 ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new start of Ao and possible cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high, and $\overline{CS}$ is low. That data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:

BYTE 1

| X X X X | X X X X |

MSB

BYTE 2

| X X X X | O O O O |

LSB

This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the address bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is completed and STS is low. If earlier access is needed, the read can begin no later than the addition of time t_{DD} and t_{HS} before STS goes low.

Figure 14 - Control Logic

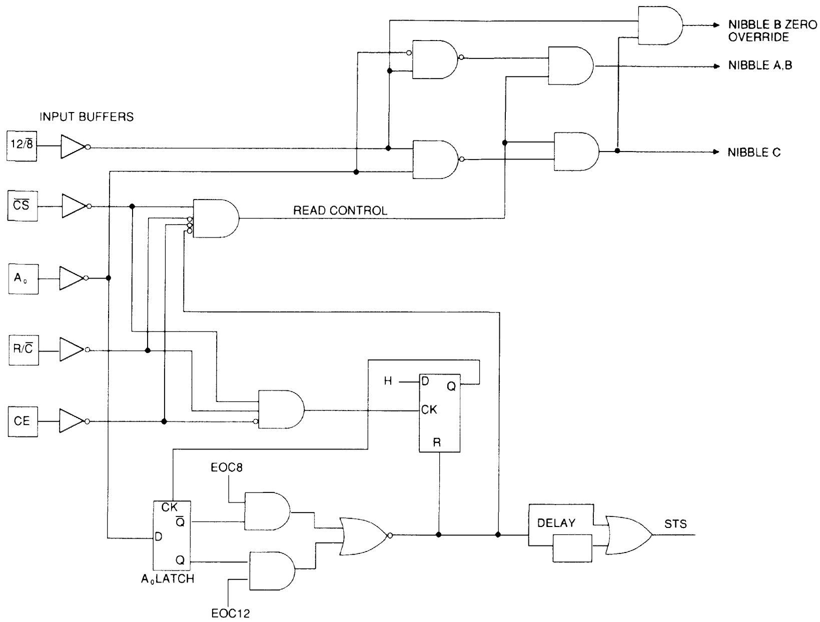
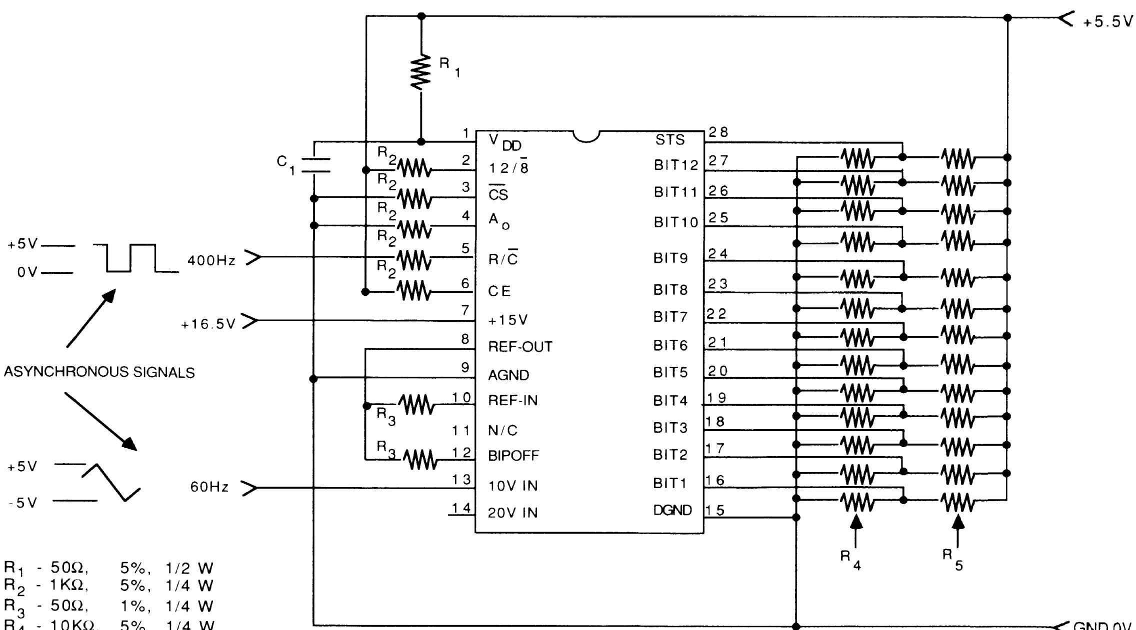
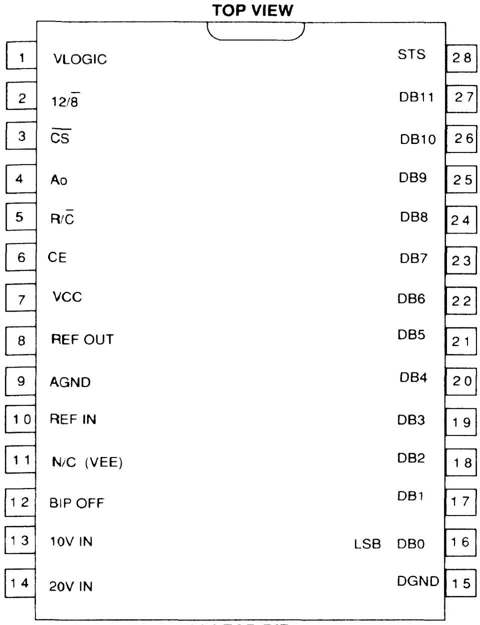


Figure 15 - Burn-In Schematic

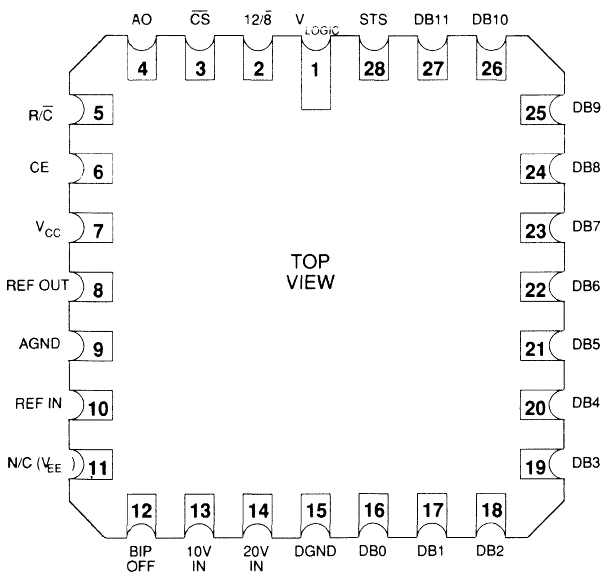


R_1 - 50Ω, 5%, 1/2 W
R_2 - 1KΩ, 5%, 1/4 W
R_3 - 50Ω, 1%, 1/4 W
R_4 - 10KΩ, 5%, 1/4 W
R_5 - 3.3KΩ, 5%, 1/4 W
C_1 - 1μF, 5%

PIN Assignment SPT774



28 LEAD DIP



PIN Functions SPT774

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5 V
12/$\overline{8}$	Data Mode Selection
$\overline{CS}$	Chip Selection
Ao	Byte Address/Short Cycle
R/$\overline{C}$	Read/Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage, Nominally +15 V
REF OUT	Reference Output, Nominally +10 V
AGND*	Analog Ground
REF IN	Reference Input
N/C (V_{EE})	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10 V IN	10 Volt Analog Input
20 V IN	20 Volt Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

* The lid on the sidebrazed and LCC packages are internally connected to AGND.

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

SPT7572

COMPLETE HIGH-SPEED 12-BIT A/D CONVERTER

ADVANCE INFORMATION

3

FEATURES

- Improved Version of the AD7572
- 12-Bit Resolution and Accuracy
- High Speed; 5 and 12.5 µsec Versions
- Improved Analog Input Circuitry;
  No Dynamic Source Loading
  High Impedance
- Improved Negative Power Supply Range;
  -10.5 to -16.5 Volts
- Lower Power: 150 mW Max

APPLICATIONS

- Data Acquisition
- Instrumentation
- Process Control
- DSP System Digitizer
- Microprocessor Interface
- Personal Computer Interface

GENERAL DESCRIPTION

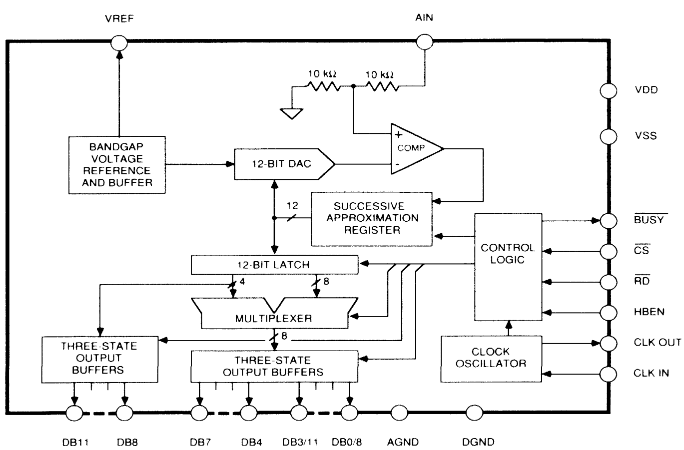
The SPT7572 is a complete 12-bit A/D converter that offers high speed with low power dissipation. This is achieved with a successive approximation architecture on a monolithic BI-MOS process. Unlike the AD7572, the SPT7572 uses analog input circuitry that reduces the amount of kickback, or synchronous noise, to the driver source during the conversion. This minimizes the required bandwidth of the circuitry driving the SPT7572, lowers the system cost and simplifies system design.

The SPT7572 also offers an improved negative power supply range of -10.5 to -16.5 volts. This broadens application possibilities and simplifies applications that utilize negative power supplies which vary from the standard -15 volt analog supply system.

The pretrimmed internal bandgap voltage reference assures stable operation over all operating conditions. Device timing is controlled by the external synchronous clock input, or an optional external crystal. For 0 to 5 volt unipolar operation, no external components are required. Decoupling capacitors at the power supply pins are recommended.

The tri-state data outputs and high speed digital interface of the SPT7572 ensures compatibility with most popular 8, 16 and 32-bit microprocessors. The device is packaged in a 24-pin 300 mil DIP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) 25 °C

Supply Voltages

V_{DD} to DGND ....-0.3 V to +7 V
V_{SS} to DGND ....+0.3 V to -17 V
AGND to DGND ....-0.3 V, V_{DD} +0.3 V
AIN to AGND ....±15 V

Input Voltages

Digital Input Voltage to DGND
(CLK IN, HBEN, $\overline{RD}$, $\overline{CS}$ ....-0.3 V, V_{DD} + 0.3 V

Output Voltages

Digital Output Voltage to DGND
(D11-D0/8, CLK OUT, $\overline{BUSY}$) ....-0.3 V, V_{DD} +0.3 V

Temperature

Operating Temperature ....0 to +70 °C
Lead Temperature ....+300 °C
Storage Temperature ....-65 °C to +150 °C
Power Dissipation...1000 mW
Derates above +75 °C by................................10 mW/°C

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

V_{DD} = 5 V, V_{SS} = -15 V, ƒCLK: 2.5 MHz for SPT7572XXX05, 1 MHz for SPT7572XXX12.
All Specification T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT7572A MIN	SPT7572A TYP	SPT7572A MAX	SPT7572B MIN	SPT7572B TYP	SPT7572B MAX	SPT7572C MIN	SPT7572C TYP	SPT7572C MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
ACCURACY												
Resolution					12			12			12	Bits
Integral Nonlinearity		I			±1/2			±1			±1	LSB
Differential Nonlinearity		I			±1			±1			±1	LSB
Minimum Resolution for which no Missing Codes are Guaranteed					12			12			12	Bits
Offset Error @ +25 °C		I			±3			±3			±4	LSB
T_{min} to T_{max}	Typical Change over Temp is = ±0.5 LSB	I			±4			±5			±6	LSB
Full Scale (FS) Error[1]	V_{DD}=5 V, V_{SS}=-15 V, FS = 5 V, T_A=+25 °C	I			±10			±10			±15	LSB
Full Scale TC[2,3]	Ideal Last Code Transition = FS - 3/2 LSBs	I			25			25			45	ppm/°C
ANALOG INPUT												
Input Voltage Range		I	0		+5	0		+5	0		+5	Volts
Input Current		I		0.3	0.7		0.3	0.7		0.3	0.7	mA
INTERNAL REFERENCE VOLTAGE												
V_{REF} Output @ +25 °C		I	-5.2		-5.3	-5.2		-5.3	-5.2		-5.3	Volts
V_{REF} Output TC		V		20			20			40		ppm/°C
Output Current Sink Capability	External Load Should Not Change During Conversion	I			550			550			550	μA

ELECTRICAL SPECIFICATIONS

V_{DD} = 5 V, V_{SS} = -15 V, ƒCLK: 2.5 MHz for SPT7572XXX05, 1 MHz for SPT7572XXX12.
All Specification T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT7572A MIN	SPT7572A TYP	SPT7572A MAX	SPT7572B MIN	SPT7572B TYP	SPT7572B MAX	SPT7572C MIN	SPT7572C TYP	SPT7572C MAX	UNITS
POWER SUPPLY REJECTION												
V_{DD} Only	FS Change, VSS=-15 V, V_{DD} = +4.75 V to +5.25 V	II		±1/2			±1/2			±1/2		LSB
V_{SS} Only	FS Change, VDD=5 V, V_{SS} = -11.4 V to -15.75 V	II		±1/2			±1/2			±1/2		LSB
DIGITAL CHARACTERISTICS												
LOGIC INPUTS												
$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN												
V_{INL}, Input Low Voltage		I			+0.8			+0.8			+0.8	Volts
V_{INH}, Input High Voltage		I	+2.4			+2.4			+2.4			Volts
C_{IN}, Input Capacitance		IV			10			10			10	pF
$\overline{CS}$, $\overline{RD}$, HBEN												
I_{IN}, Input Current	V_{IN} = 0 to V_{DD}	I			±10			±10			±10	μA
CLK IN												
I_{IN}, Input Current	V_{IN} = 0 to V_{DD}	I			±20			±20			±20	μA
LOGIC OUTPUTS												
CLK OUT												
V_{OL}, Output Low Voltage	I_{SINK} = 1.0 mA	I			+0.4			+0.4			+0.4	Volts
V_{OH}, Output High Voltage	I_{SOURCE} = 200 μA	I	+4.0			+4.0			+4.0			Volts
D11-D0/8, $\overline{BUSY}$												
V_{OL}, Output Low Voltage	I_{SINK} = 1.6 mA	I			+0.4			+0.4			+0.4	Volts
V_{OH}, Output High Voltage	I_{SOURCE} = 200 μA	I	+4.0			+4.0			+4.0			Volts
D11-D0/8												
Floating State Leakage Current		I			±10			±10			±10	μA
Floating State Output Capacitance		IV			15			15			15	pF
CONVERSION TIME[4]												
SPT7572XXX05												
Synchronous Clock	f_{CLK} = 2.5 MHz	I			5			5			5	μs
Asynchronous Clock			4.8		5.2	4.8		5.2	4.8		5.2	μs
SPT7572XXX12												
Synchronous Clock	f_{CLK} = 1 MHz	I			12.5			12.5			12.5	μs
Asynchronous Clock			12		13	12		13	12		13	μs

V_{DD} = 5 V, V_{SS} = -15 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT7572A MIN	SPT7572A TYP	SPT7572A MAX	SPT7572B MIN	SPT7572B TYP	SPT7572B MAX	SPT7572C MIN	SPT7572C TYP	SPT7572C MAX	UNITS
POWER REQUIREMENTS												
V_{DD}		I	4.75	+5	5.25	4.75	+5	5.25	4.75	+5	5.25	Volts
V_{SS}		I	-10.5	-15	-16.5	-10.5	-15	-16.5	-10.5	-15	-16.5	Volts
I_{DD}	AIN=5 V;$\overline{CS}$=$\overline{RD}$=V_{DD}	I		9	15		9	15		9	15	mA
I_{SS}	AIN=5 V;$\overline{CS}$=$\overline{RD}$=V_{DD}	I		3	5		3	5		3	5	mA
Power Dissipation				100	150		100	150		100	150	mW
TIMING CHARACTERISTICS [5]												
t_1 $\overline{CS}$ to $\overline{RD}$ Setup Time		III	0			0			0			ns
t_2 $\overline{RD}$ to $\overline{BUSY}$ Propagation Delay		III		45	230		45	230		45	230	ns
t_3[6] Data Access Time after $\overline{RD}$, CL =20 pF		III		50	110		50	110		50	110	ns
Data Access Time after $\overline{RD}$, CL = 100 pF		III		60	150		60	150		60	150	ns
t_4 $\overline{RD}$ Pulse Width		III	t3			t3			t3			ns
t_5 $\overline{CS}$ to $\overline{RD}$ Hold Time		III	0			0			0			ns
t_6[6] Data Setup Time after $\overline{BUSY}$		III		40	90		40	90		40	90	ns
t_7[7] Bus Relinquish Time		III	20	40	75	20	40	75	20	40	75	ns
t_8 HBEN to $\overline{RD}$ Setup Time		III	0			0			0			ns
t_9 HBEN to $\overline{RD}$ Hold Time		III	0			0			0			ns
t_{10} Delay Between Successive Read Operations		III	200			200			200			ns

Specifications subject to change without notice.

NOTES:

[1]Includes internal voltage reference error.

[2]Full-Scale TC = ΔFS/ΔT, where ΔFS is Full-Scale change from T_A = +25 °C to T_{min} or T_{max}.

[3]Includes internal voltage reference drift.

[4]Conversion time is measured at specified frequency with falling edge of $\overline{RD}$ coincident to the falling edge of CLK OUT.

[5]Timing Specifications are sample tested at +25 °C to ensure compliance. All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[6]t_3 and t_6 are measured with the load circuits of Figure 5 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[7]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 6.

TEST LEVEL CODES

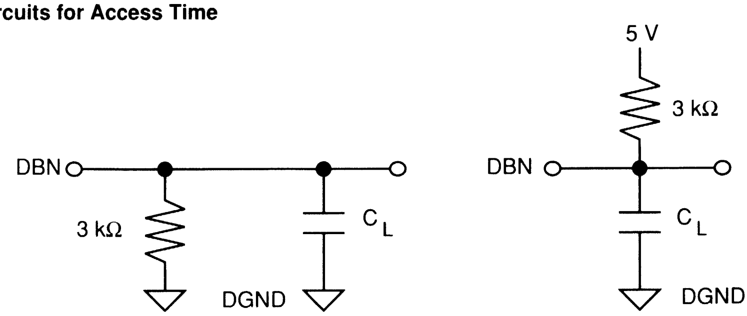
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

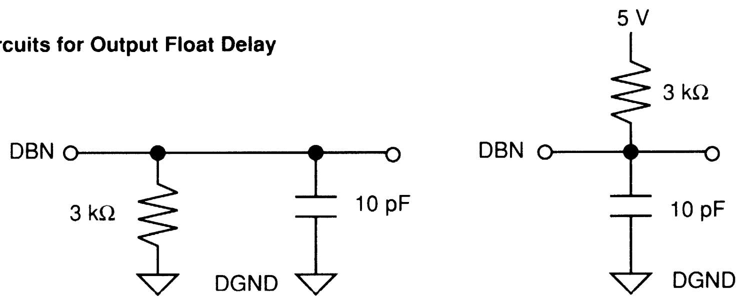
Figure 1 - Load Circuits for Access Time



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 2 - Load Circuits for Output Float Delay



a. V_{OH} to High-Z

b. V_{OL} to High-Z

CIRCUIT OPERATION

The SPT7572 is a complete high-speed 12-bit analog-to-digital converter. The monolithic design contains a 12-bit DAC with voltage reference, comparator, successive approximation register (SAR), clock, output buffers and control circuitry to ensure compatibility with most 8, 16, and 32 microprocessors.

When the control section of the SPT 7572 initiates a conversion, the successive approximation register is reset and data output buffers enabled. A conversion cycle cannot be restarted once it has begun.

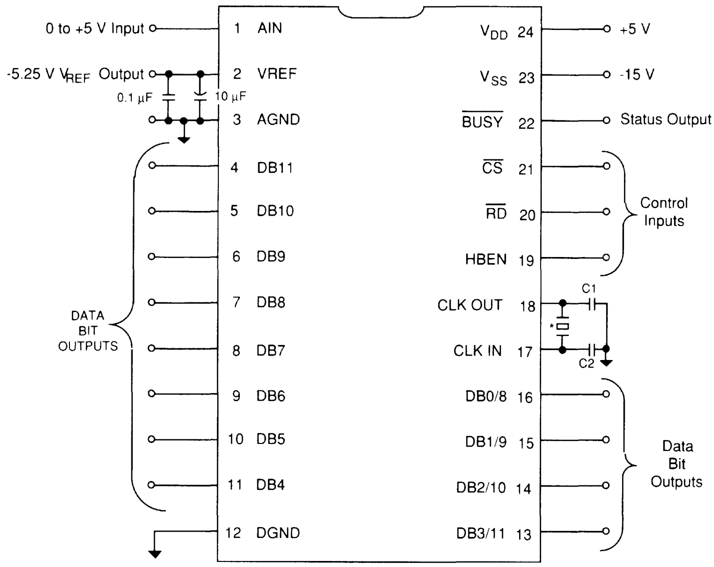
The internal 12-bit DAC is sequenced by the SAR starting from the MSB to the LSB during conversion. After testing all the bits, a 12-bit binary code is contained in the SAR accurately representing the input signal. Control logic then enables the SAR contents to be loaded in the 12-bit latch for transfer to the output buffers.

The SPT7572 has a pretrimmed internal bandgap voltage reference and buffer to assure stable operation over all temperature ranges. The reference is internally connected to the DAC and can supply up to 550 µA to an external load.

CALIBRATION AND CONNECTION PROCEDURES

Figure 3 is an operational diagram showing the minimum external configuration for the SPT7572 to perform an analog-to-digital conversion. Note that the only external components required are a crystal/ceramic resonator and four capacitors.

Figure 3 - Operational Diagram



* 2.5 MHz resonator for 5 μs device
1.0 MHz resonator for 12.5 μs device
C1 and C2 values depend on characteristics of resonator. Typical values are 30 to 100 pF.

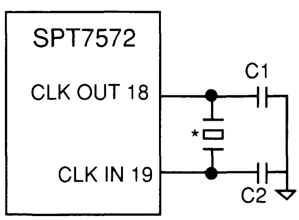
CONTROL INPUTS SYNCHRONIZATION

Data conversion time for the SPT7572 can vary from 12 to 13 clock cycles in applications in which the ADC clock and $\overline{RD}$ control input are not in sync. The 12 to 13 clock cycles are the result of the ADC waiting for the first falling CLK IN edge after conversion start before conversion begins. This means a worst case delay is an entire conversion cycle if $\overline{RD}$ and clock are not synchronized. If the application requires constant conversion time, $\overline{RD}$ must move low on the rising edge of CLK IN or the falling edge of CLK OUT.

INTERNAL CLOCK OSCILLATOR

Figure 4 shows the proper connection of an external crystal or ceramic resonator to the SPT7572 to provide a clock oscillator. ADC timing is achieved by the 50% duty cycle of the oscillator between CLK IN and CLK OUT. The resonator can be omitted if an external clock source with a 50% duty cycle is connected to CLK IN with an inverted CLK IN signal at CLK OUT.

Figure 4 - Internal Clock Oscillator



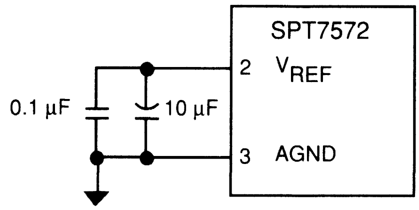
* 2.5 MHz oscillator for 5 μs device
1.0 MHz oscillator for 12.5 μs device
C1 and C2 values depend on characteristics of the oscillator. Typically 30 to 100 pF.

INTERNAL BANDGAP REFERENCE

The SPT7572 has an internal bandgap reference trimmed to -5.25 V. Pin 2 is the V_{REF} output which makes up to 550 µA of current available to an external load with .

If V_{REF} is used, a decoupling capacitor should be used to filter noise. Large capacitor values, however, will affect the dynamic response and stability of the reference. A recommended schematic for decoupling is shown in Figure 5.

Figure 5 - Decoupling Schematic

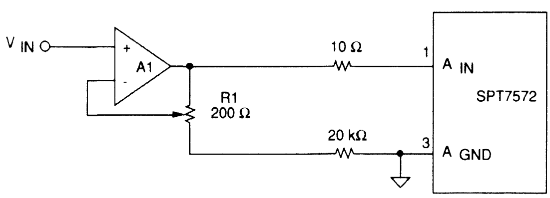


UNIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

Figure 6 shows the interfacing circuit for unipolar offset and full-scale error adjustment. This configuration allows for offset and full-scale error to be adjusted to zero. (Offset is adjusted before full scale.)

Considering zero offset error, an input of +0.5 LSB (0.61 mV) is applied to V_{IN}. The op amp is adjusted for code transition changes at the ADC output between 0-00 and 0-01. Zero full-scale error adjustment is done by applying an input of 4.99817 V (FS-3/2 LSBs) to V_{IN} and adjusting R1 until the ADC output code transitions change between 1-10 and 1-11.

Figure 6 - Unipolar 0 to +5 V Operation with Gain Error Adjust

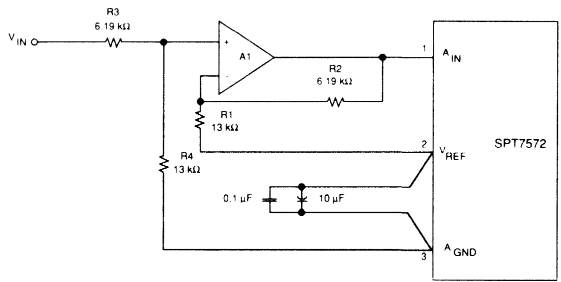


BIPOLAR OPERATION, OFFSET BINARY AND COMPLEMENTARY OFFSET BINARY OUTPUT CODE

Bipolar operation with offset binary output code is achieved using the circuit configuration shown in Figure 8. An op-amp is used to offset V_{IN} by 2.5 V. The transfer function for this circuit is A_{IN}=VIN +2.5 V. The analog input range is ±2.5 V with an LSB=1.22 mV.

Values of R3 and R4 can adjusted for other input signal ranges. All resistors should be the same type and be made by the same manufacturer so that temperature coefficients match. The resistors should be chosen so the full dynamic range of the ADC (0 to 5 V) is covered at AIN.

Figure 7 - Bipolar Operation, Output Code offset Binary

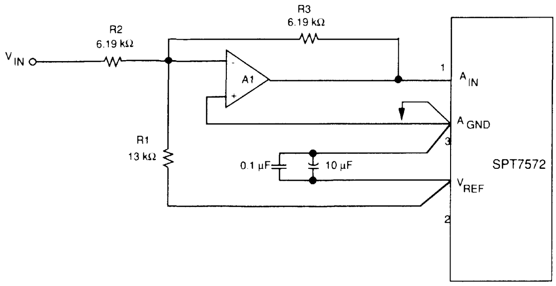


BIPOLAR OPERATION, OUTPUT CODE COMPLEMENTARY OFFSET BINARY

Bipolar operation with complementary offset binary output code is achieved using the circuit configuration shown in Figure 8. An op-amp is used to offset V_{IN} by 2.5 V. The transfer function for this circuit is AIN = $-V_{IN}$+2.5 V. The analog input range is ±2.5 V with an LSB of 1.22 mV.

R2 can be adjusted for other input signal ranges. All resistors should be the same type and manufacturer so temperature coefficients match. The resistors should be chosen so the full dynamic range of the ADC (0 to 5 V) is covered at AIN.

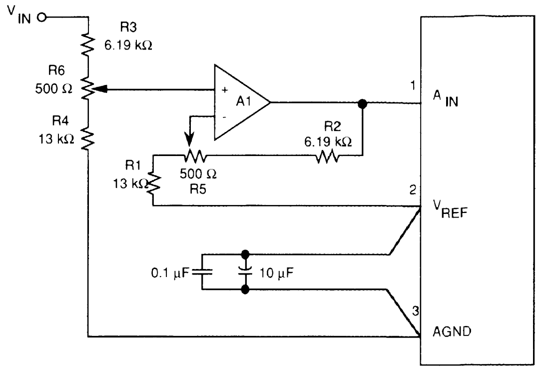
Figure 8 - Bipolar Operation, Output Code Offset Binary



BIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

Offset and full-scale errors can be adjusted using the circuit shown in Figure 9. Offset is adjusted before full-scale error. The offset is adjusted by applying .61 mV to V_{IN} and tuning R5 until the output code changes between 10-00 and 10-01. The full-scale error is adjusted by applying 2.49817 volts (last transition point) and tuning R6 until the output code changes between 1-10 and 1-11.

Figure 9 - Bipolar Operation with Offset and Gain Error Adjust



TIMING AND CONTROL

DATA FORMAT

The SPT7572 can provide output data in parallel or two-byte load for 16-bit and 8-bit microprocessors, respectively. The LSB is always right justified in the digital word. In the two byte read mode, DB7...DB0/8 are used while DB11...DB8 are ignored. High byte enable (HBEN) controls the digital multiplexer so that data can be read in two cycles in 8-bit systems.

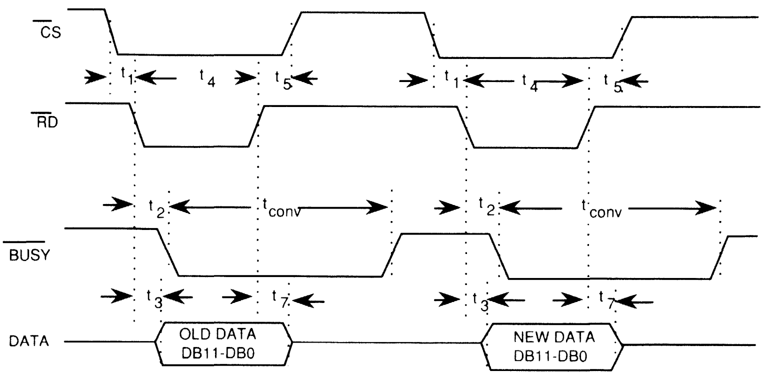
DATA BUS OUTPUT, $\overline{CS}$ AND $\overline{RD}$=LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
PIN DEFINITION	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN=LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN=HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Notes: D11...D0/8 are the ADC data output pins
DB11...DB0 are the 12-bit conversion results; DB11 is the MSB.

Figure 10 - ROM Mode, Parallel Read Timing and Data Status Diagram.

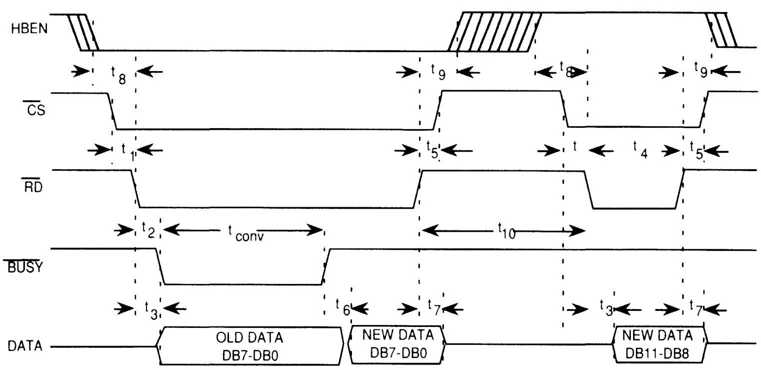
This eliminates the need for the microprocessor to move into a wait state. This mode allows data to be disregarded if not needed during a given time period, keeping the CPU out of a wait state. When the SPT7572 minimum conversion time has elapsed, another READ operation begins. This sequence continues as long as the $\overline{CS}$ and $\overline{RD}$ logic initiate READ operations.



DATA OUTPUTS	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Figure11 - Slow Memory Mode, Two Byte Read Timing Diagram

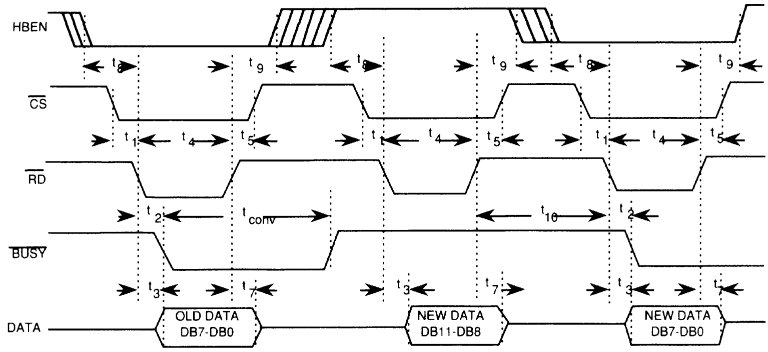
Figure 11 is the timing and data output status diagram for the slow memory mode, two byte read. For this application, only data outputs D7 ... D0/8 are used. Conversion begins in the same manner as the slow memory mode, parallel read. New data is placed on the data bus, but only the lower 8-bits (D7 ... D0) are read from the ADC. HBEN is moved high to signal a second READ, placing the high 4-bits on D3/ ... D0/8. During the two READ operations, the four MSBs appear on data outputs D11 ... D8.



DATA OUTPUTS	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8

Figure 12 - ROM Mode, Two Byte Read Timing Diagram

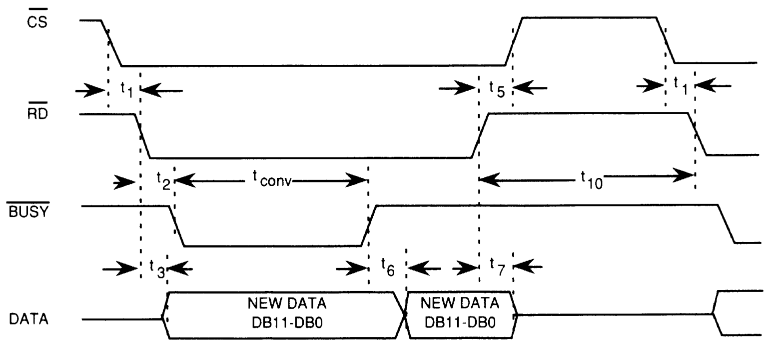
Figure 12 is the ROM mode, two byte read timing and data status diagram. In this mode, the data outputs are segmented using D7 ... D0/8. The four MSBs are placed on the data bus first, on D3/11 ... D0/8, followed by the lower 8-bits. This sequence is opposite the slow memory mode, two byte READ.



DATA OUTPUTS	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

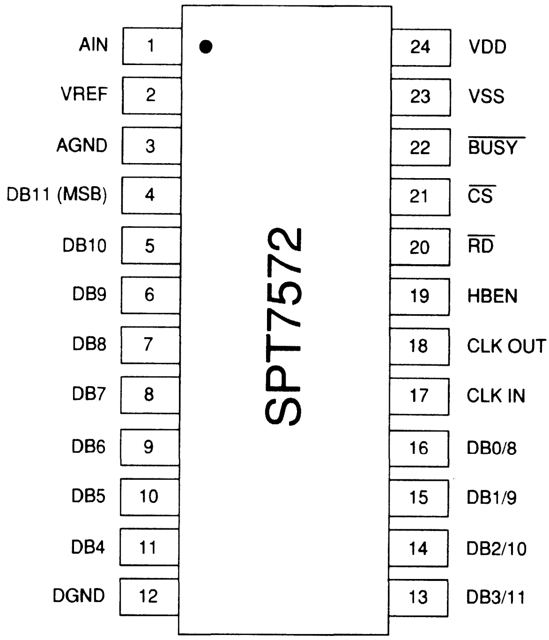
Figure 13 - Slow Memory Mode, Parallel Read Timing Diagram

Figure 13 is the data bus status and timing diagram for the slow memory mode, parallel read. A data conversion is triggered by $\overline{CS}$ and $\overline{RD}$ going low. The SPT7572 acknowledges this conversion by taking $\overline{BUSY}$ low. The three-state data outputs hold data from the previous conversion. At the end of the conversion when output latches have been updated, $\overline{BUSY}$ returns high and the conversion result is placed on data outputs D11...D0/8.



DATA OUTPUTS	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

PIN ASSIGNMENT SPT7572



PIN FUNCTIONS

NAME	FUNCTION
AIN	Analog Input
VREF	Voltage Reference Output
AGND	Analog Ground
DB11	Data Bit 11, Active when $\overline{CS}$ and $\overline{RD}$ are low
DB10	Data Bit 10, Active when $\overline{CS}$ and $\overline{RD}$ are low
DB9	Data Bit 9, Active when $\overline{CS}$ and $\overline{RD}$ are low
DB8	Data Bit 8, Active when $\overline{CS}$ and $\overline{RD}$ are low
DB7	Data Bit 7, Active when $\overline{CS}$ and $\overline{RD}$ are low
DB6	Data Bit 6, Active when $\overline{CS}$ and $\overline{RD}$ are low
DB5	Data Bit 5, Active when $\overline{CS}$ and $\overline{RD}$ are low
DB4	Data Bit 4, Active when $\overline{CS}$ and $\overline{RD}$ are low
DGND	Digital Ground
DB3/11	Data Bit 3/11, Changes with status of HBEN
DB2/10	Data Bit 2/10, Changes with status of HBEN
DB1/9	Data Bit 1/9, Changes with status of HBEN
DB0/8	Data Bit 0/8, Changes with status of HBEN
CLK IN	Clock Input
CLK OUT	Clock Output
HBEN	High Byte Enable Input
$\overline{RD}$	Read Input
$\overline{CS}$	Chip Select Input
$\overline{BUSY}$	Busy Output
V_{SS}	Negative Supply -15 V
V_{DD}	Positive Supply +5 V

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

HADC77100

8-BIT, 150 MSPS FLASH A/D CONVERTER

FEATURES

- 150 MSPS Conversion Rate
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Typical Power Dissipation < 2.2 Watts

APPLICATIONS

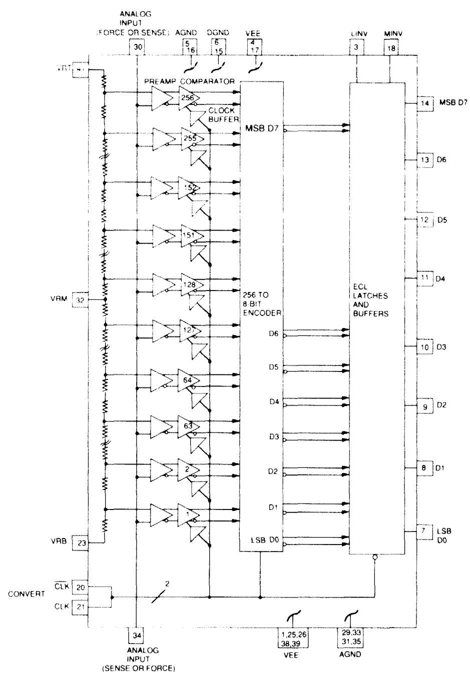
- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The HADC77100 is a monolithic flash A/D converter capable of digitizing a two volt analog input signal with full scale frequency components to 50 MHz into 8-bit digital words at a 150 MSPS (TYP) update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time and wide bandwidth. A single standard -5.2 volt power supply is required for operation of the HADC77100, with nominal power dissipation of 2.2 Watts. The part is packaged in a 42 Lead Ceramic Sidebrazed DIP which is pin compatible with the CX20116. Careful attention to the design and layout has provided a device with better linearity, lower noise floor, stable input characteristics, and lower data error rates. The HADC77100 is available in industrial and military temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
Negative Supply Voltage (V_{EE} TO GND) .... -7.0 to +0.5 V
Ground Voltage Differential .... -0.5 to +0.5 V

Input Voltage
Analog Input Voltage .... +0.5 V to V_{EE}
Reference Input Voltage .... +0.5 V to V_{EE}
Digital Input Voltage .... +0.5 V to V_{EE}
Reference Current VRT to VRB .... 25 mA

Output
Digital Output Current .... 0 to -25 mA

Temperature
Operating Temperature, ambient .... -65 to +105 °C
case .... +125 °C
junction .... +150 °C
Lead Temperature, (soldering 10 seconds). .... +300 °C
Storage Temperature .... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_C=T_{CASE}=+125 °C, T_A=$T_{AMBIENT}$, V_{EE}=-5.2 V, R_{Source} =10 Ω, VRB=-2.00 V, VRT=0.00 V, f_{clk}=100 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25 °C MIN	ROOM +25 °C TYP	ROOM +25 °C MAX	HOT T_{MAX} MIN	HOT T_{MAX} MAX	COLD T_{MIN} MIN	COLD T_{MIN} MAX	UNITS
DC ELECTRICAL CHARACTERISTICS										
Integral Linearity, 77100A	T_A = -25 to +85 °C	II			±1/2		±1/2		±1/2	LSB
	T_A = -55 to T_C	I			±1/2		±3/4		±3/4	LSB
Differential Linearity, 77100A (No missing codes)	T_A = -25 to +85 °C	II			±1/2		±1/2		±1/2	LSB
	T_A = -55 to T_C	I			±1/2		±3/4		±3/4	LSB
Integral Linearity, 77100B		II			±3/4		±3/4		±3/4	LSB
Differential Linearity, 77100B (No missing codes)		II			±3/4		±3/4		±3/4	LSB
Offset Error VRT	T_A = -25 to +85 °C	II			±30		±30		±30	mV
	T_A = -55 to T_C	I			±30		±30		±30	mV
Offset Error VRB	T_A = -25 to +85 °C	II			±30		±30		±30	mV
	T_A = -55 to T_C	I			±30		±30		±30	mV
Input Voltage Range	T_A = -25 to +85 °C	II	-2.0		0.0	-2.0	0.0	-2.0	0.0	Volts
	T_A = -55 to T_C	I	-2.0		0.0	-2.0	0.0	-2.0	0.0	Volts
Input Capacitance	Over full input range	V		45						pF
Input Resistance		V		100						kΩ
Input Current	T_A = -25 to +85 °C	II		300	500		450		650	µA
	T_A = -55 to T_C	I		300	500		400		750	µA
Clock Synchronous Input Currents		V		40						µA
Supply Current	T_A = -25 to +85 °C	II		420	505		525		505	mA
	T_A = -55 to T_C	I		420	505		535		505	mA
Power Dissipation		II		2.18	2.63		2.73		2.63	mA
Ladder Resistance	T_A = -25 to +85 °C	II	100		300	100	300	80	300	Ω
	T_A = -55 to T_C	I	100		300	130	300	60	300	Ω
Reference Bandwidth		V		50						MHz

ELECTRICAL SPECIFICATIONS

T_C=T_{CASE}=+125 °C, T_A=$T_{AMBIENT}$, V_{EE}=-5.2 V, R_{Source} =10 Ω, VRB=-2.00 V, VRT=0.00 V, f_{clk}=100 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	LEVEL	ROOM +25 °C MIN	ROOM +25 °C TYP	ROOM +25 °C MAX	HOT T_{MAX} MIN	HOT T_{MAX} MAX	COLD T_{MIN} MIN	COLD T_{MIN} MAX	UNITS
DIGITAL CHARACTERISTICS										
Output High Voltage	50 Ω to -2 V									
	T_A = -25 to +85 °C	II	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	Volts
	T_A = -55 to T_C	I	-0.98	-0.90	-0.82	-0.85	-0.66	-1.10	-0.95	Volts
Output Low Voltage	50 Ω to -2 V									
	T_A = -25 to +85 °C	II	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	Volts
	T_A = -55 to T_C	I	-1.95	-1.80	-1.65	-1.95	-1.65	-2.00	-1.70	Volts
Input High Voltage (MINV, LINV)	T_A = -25 to +85 °C	II	-1.13		-0.81	-1.07	-0.67	-1.19	-0.87	Volts
	T_A = -55 to T_C	I	-1.13		-0.81	-1.07	-0.67	-1.22	-0.87	Volts
Input Low Voltage (MINV, LINV)	T_A = -25 to +85 °C	II	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	Volts
	T_A = -55 to T_C	I	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	Volts
AC ELECTRICAL CHARACTERISTICS										
Maximum Sample Rate	T_A = -25 to +85 °C	IV	125	150		125		125		MSPS
	T_A = -55 to T_C	I	100	150		100		100		MSPS
Clock Low Width, TPW0	T_A = -25 to +85 °C	II	5	3						ns
	T_A = -55 to T_C	I	5	3		5		5		ns
Clock High Width, TPW1	T_A = -25 to +85 °C	II	5	3						ns
	T_A = -55 to T_C	I	5	3		5		5		ns
Output Delay, TD	Differential Clock	V	3	4.2	5					ns
Output Delay Tempco	Differential Clock	V		15						ps/°C
Large Signal Bandwidth	Vin = F.S.	V		100						MHz
Small Signal Bandwidth	Vin=500 mV PP	V		175						MHz
Aperture Jitter		V		12						ps
Aperture Delay	Differential Clock T_A = -25 to +85 °C	V	0.3	1.8	2.3					ns
Aperture Delay Tempco	Differential Clock	V		4						ps/°C
Aperture Time		V		<100						ps
Acquisition Time	F.S. to ±1/2 LSB	V		5						ns
Input Slew Rate		V		800						V/μs
Total Dynamic Error	Vin = FS @ 3.58 MHz									
	T_A = -25 to +85 °C	I	44.2	48						dB
	T_A = -55 to T_C	I	44.2	48		43.2		43.5		dB
Total Dynamic Error, 77100A	Vin = FS @ 50 MHz									
	T_A = -25 to +85 °C	I	28.2	33						dB
	T_A = -55 to T_C	I	28.2	33		27		27		dB
Signal to Noise Ratio	Vin = FS @ 3.58 MHz									
	T_A = -25 to +85 °C	I	46	49						dB
	T_A = -55 to T_C	I	46	49		45		45		dB

ELECTRICAL SPECIFICATIONS

T_C=T_{CASE}=+125 °C, T_A=$T_{AMBIENT}$, V_{EE}=-5.2 V, R_{Source} =10 Ω, VRB=-2.00 V, VRT=0.00 V, f_{clk}=100 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25 °C MIN	ROOM +25 °C TYP	ROOM +25 °C MAX	HOT T_{MAX} MIN	HOT T_{MAX} MAX	COLD T_{MIN} MIN	COLD T_{MIN} MAX	UNITS
AC ELECTRICAL CHARACTERISTICS										
Signal to Noise Ratio, 77100A	Vin = FS @ 50 MHz									
	T_A = -25 to +85 °C	I	33	38						dB
	T_A = -55 to T_C	I	33	38		32.5		32.5		dB
Total Harmonic Distortion	Vin = FS @ 3.58 MHz									
	T_A = -25 to +85 °C	I	49							dBc
	T_A = -55 to T_C	I	49	46		48		49		dBc
Total Harmonic Dist., 77100A	Vin = FS @ 50 MHz									
	T_A = -25 to +85 °C	I	30	34						dBc
	T_A = -55 to T_C	I	30	34		27		28.5		dBc
Differential Gain	NTSC 40 IRE mod. ramp, Fc = 100 MSPS	V		1.0						%
Differential Phase	NTSC 40 IRE mod. ramp, Fc = 100 MSPS	V		.5						DEG

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

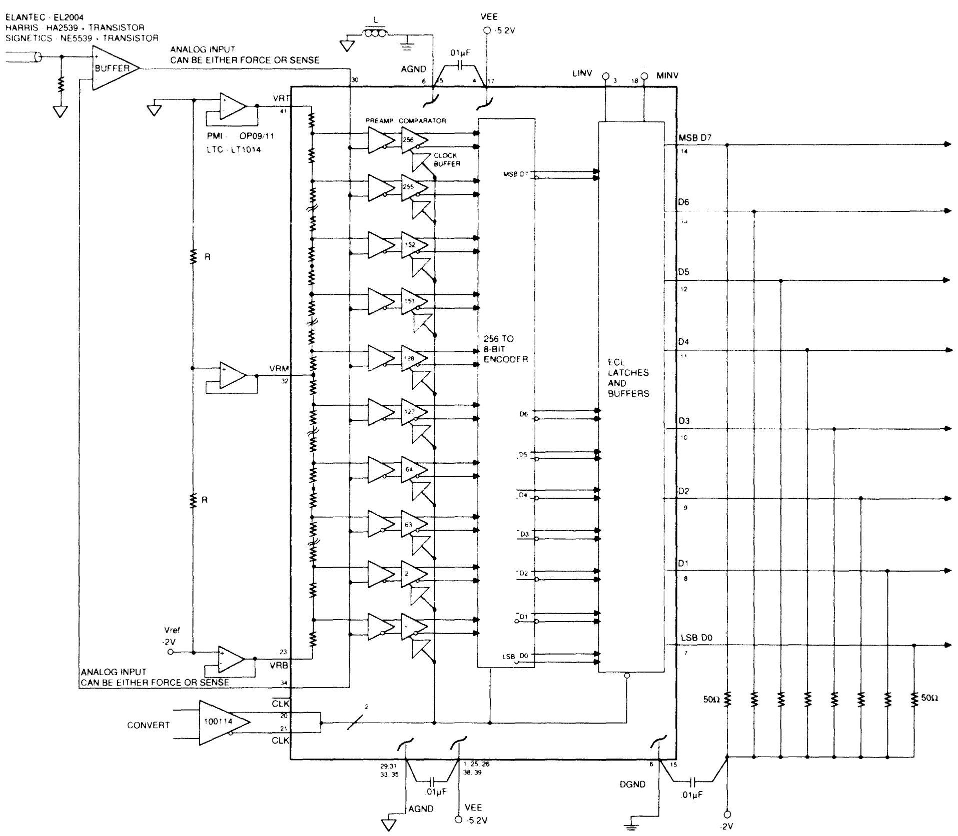
GENERAL DESCRIPTION

The HADC77100 is one of the fastest monolithic 8-bit parallel flash A/D converters available today. The nominal conversion rate is 150 MSPS and the analog bandwidth is in excess of 100 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges and therefore makes the part easier to drive than previous flash convertors. The preamplifiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The HADC77100 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77100 has an on board power supply bypass of 1500 pF to reduce external component needs. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

Figure 5 - HADC77100 Typical Interface Circuit



TYPICAL INTERFACE CIRCUIT

The HADC77100 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 5 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 5.

VIN (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force". This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77100 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836 transistor. Very high performance can be achieved by using a Comlinear CLC221/231.

CLK, $\overline{CLK}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{CLK}$ is internally biased to -1.3 V (see clock input circuit). It may be left open but a .01 µF bypass capacitor from $\overline{CLK}$ to AGND is recommended. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

MINV, LINV (OUTPUT LOGIC CONTROL)

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table II. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to AGND through a diode or 3.9 kΩ resistor.

D0 TO D7 (DIGITAL OUTPUTS)

The digital outputs can drive 50 Ω to ECL levels when pulled down to -2 V When pulled down to -5.2 V the outputs can drive 130 Ω, to 1 kΩ loads.

VRB, VRM, VRT (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are -2 V (VRB), mid-tap (VRM) and AGND (VRT). The reference pins and tap can be can be driven by op amps as shown in Figure 5 or VRM may be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression if so desired.

N/C

All "Not Connected" pins should be tied to DGND on the left side of the package and to AGND of the right side of the package.

Table II - Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

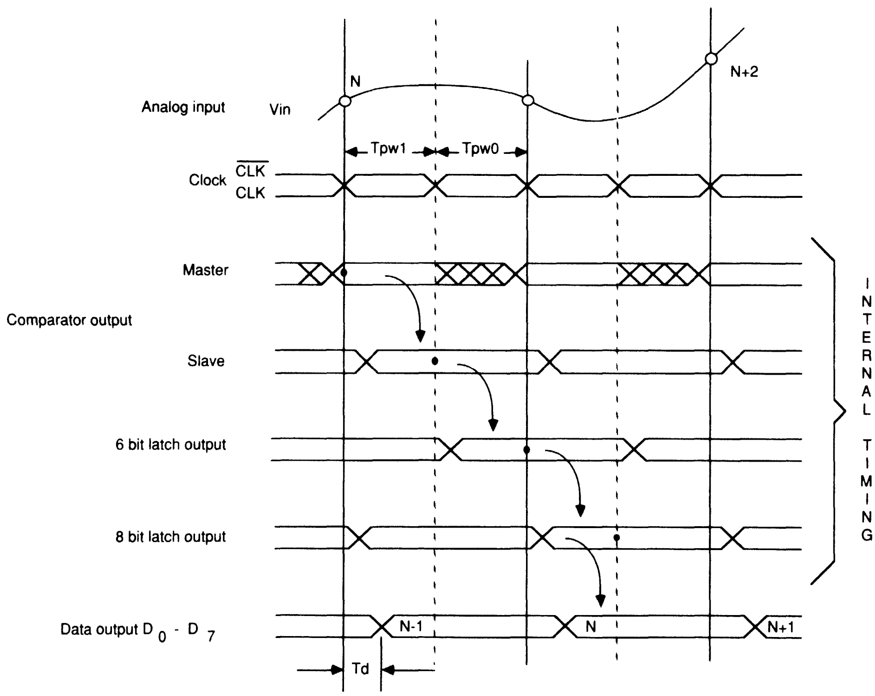
1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

OPERATION

The HADC77100 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/ comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

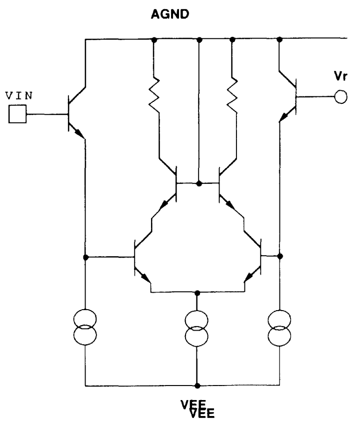
TIMING DIAGRAM



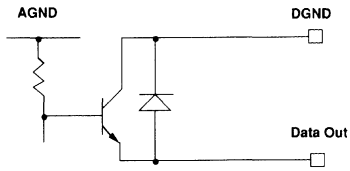
Dots (•) in the chart denote respective latch timings.

SUBCIRCUIT SCHEMATICS

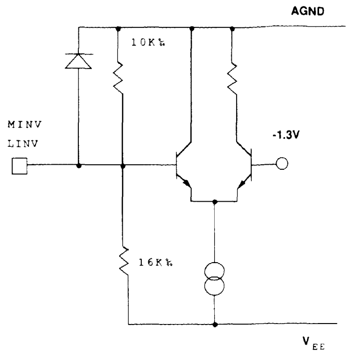
INPUT CIRCUIT



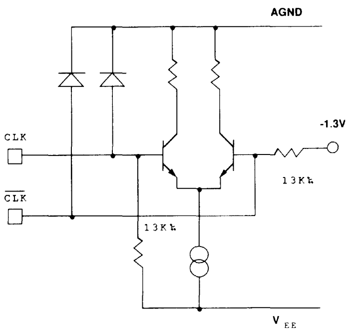
OUTPUT CIRCUIT



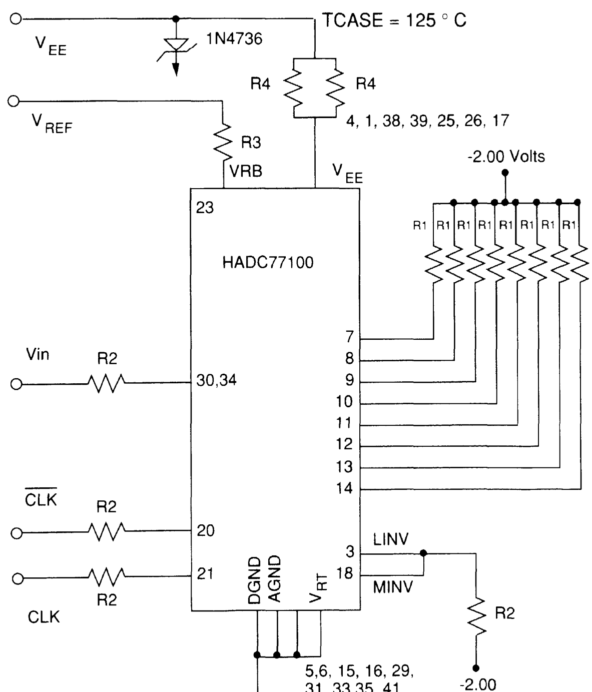
MINV, LINV INPUT CIRCUIT



CLOCK INPUT



BURN-IN CIRCUIT



R_1 = 50Ω 1/4 Watt CC 5%

R_2 = 1KΩ 1/4 Watt CC 5%

R_3 = 6.5Ω 1/4 Watt CC 5%

R_4 = 6.5Ω 1/2 Watt CC 5%

V_{REF} = -2.00 Volts

V_{EE} = -6.6 Volts

HADC77100

3

DEFINITION OF TERMS

A/D CONVERTER ERROR SUMMARY

SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 1B) while a static DC input level may appear close to the ideal (Figure 1A). That is why we are including many dynamic tests as well as the industry standard DC specifications.

TOTAL DYNAMIC ERROR (EFFECTIVE BITS)

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These errors are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from the measured RMS error for the ideal sinewave and the measured actual RMS error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual RMS error}}{\text{ideal RMS error}}$$

Furthermore, total dynamic error (TDE) can be related to effective bits by the following formula:

$$\text{TDE(dB)} = 1.8 + 6.02 \times \text{N(eff bits)}$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = FSR/2^N$ where FSR = full scale range and N = 8. Nonideal quantization bands represent differential nonlinearity errors see Figures 1A and 1B.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 1B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77100's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 1B points out two missed codes in the transfer function.

Figure 1A - Static Input Conditions

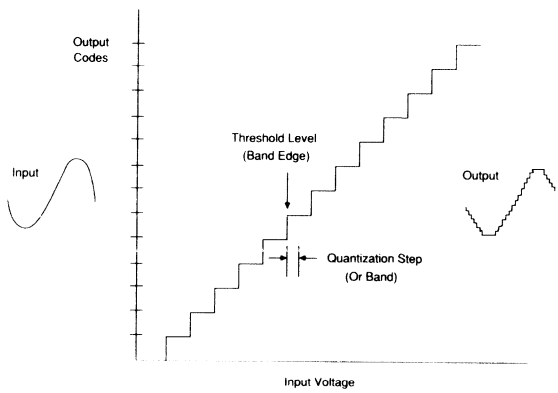
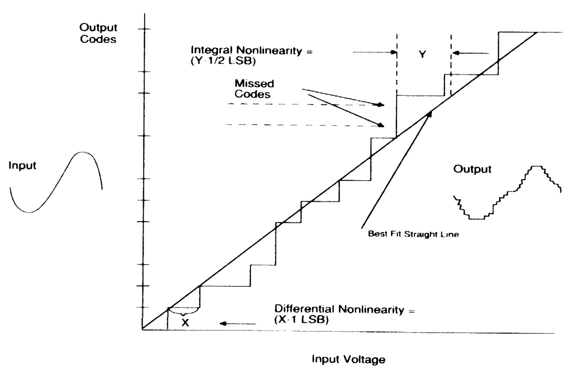


Figure 1B - Dynamic Conditions



INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 2A). Integral nonlinearity does not include any gain or offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 1B shows an integral nonlinearity error of 2 LSBs. The HADC77100's integral nonlinearity can be improved by using the external reference ladder tap as shown in Figure 5. The resulting effect on the linearity is shown in Figure 2B.

Figure 2A - Linearity Curve with no TAP adjustment

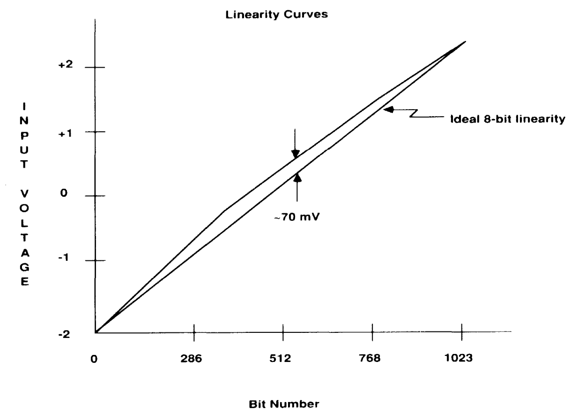
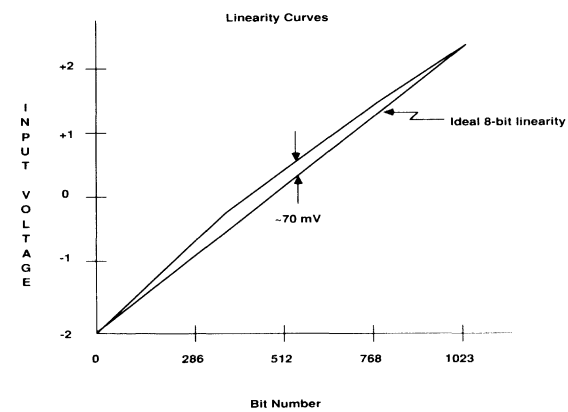


Figure 2B - Linearity Curve with TAP Forced to within .05 mV of Ideal



APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point see Figure 2C.

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sinewave can be calculated for time or voltage by the equation:

$$dV/V = 2\ \pi f t_a$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 3 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal waveforms.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10 MHz, then from Figure 3 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70 ps. Most data sheets do not state aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70 ps.

Aperture time and delay are very difficult to measure. However, these values are needed to make intelligent design decisions. SPT supplies these values for the HADC77100 based on both computer design simulations and verified by characterization of samples.

Figure 2C - Aperture Uncertainty

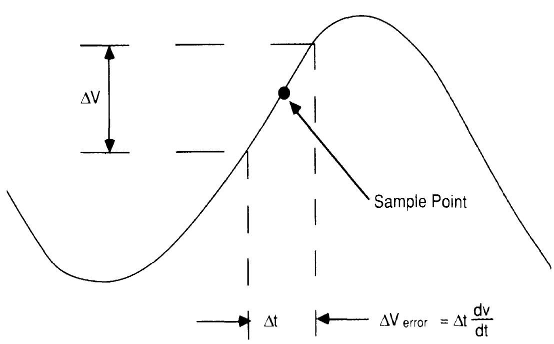
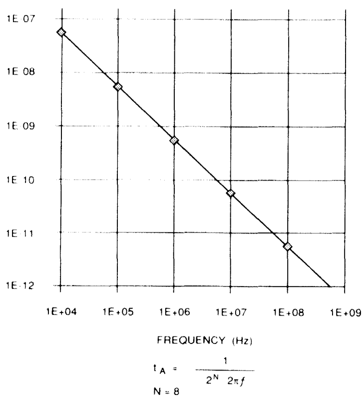


Figure 3 - Aperture Time - Sinewaves



CHARACTERISTIC TESTING

TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table 1.

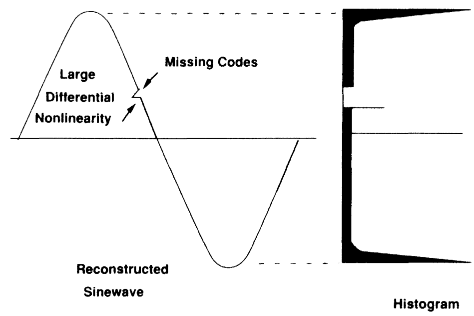
HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77100. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurrence along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{-1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurrence at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts see Figure 4.

Figure 4 - Histogram Testing



In the histogram test, the A/D transfer function step widths larger than ideal show up as "spikes" in the histogram. Codes missing from the transfer function show up as "bins" with zero counts.

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sinewave, caused by the integral nonlinearity, are aliased into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table I.

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77100. Using least squared error minimization techniques, an idealized sinewave fit to the data is calculated by software. The sinewave is in the form:

$$A\sin(2\pi ft+\theta)+DC$$

where A, f, q, DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave,

$$A_0\sin(2\pi f_0 t+\theta_0)+DC_0$$

is then subtracted from the digitized time record. The RMS errors are then calculated and the effective bits specification is found.

BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77100. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converters sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δ f, is observed. Differential nonlinearities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

DYNAMIC EVALUATION

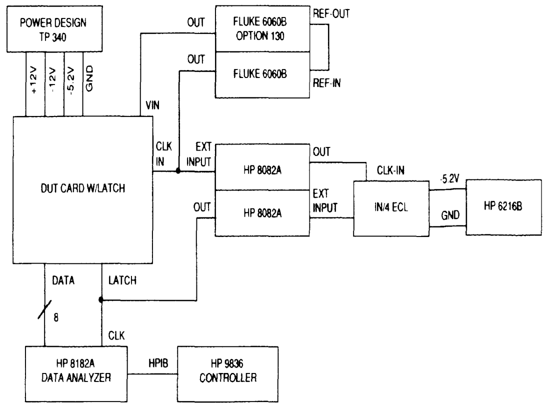


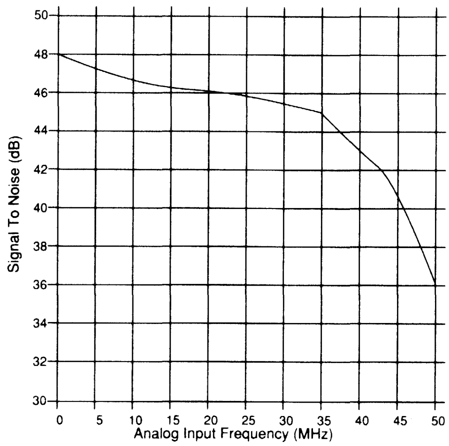
Table I - Tests

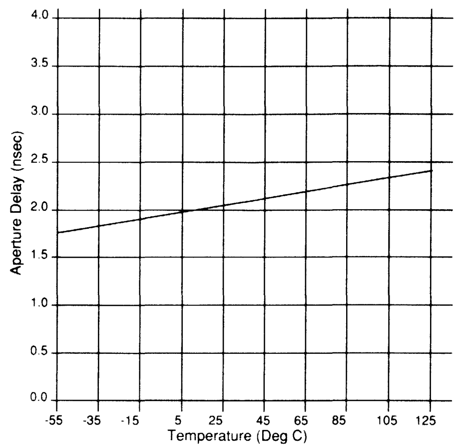
The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

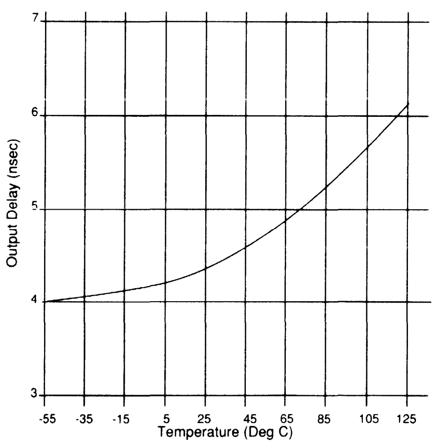
(Table from H.P. Product Note 5180A-2)

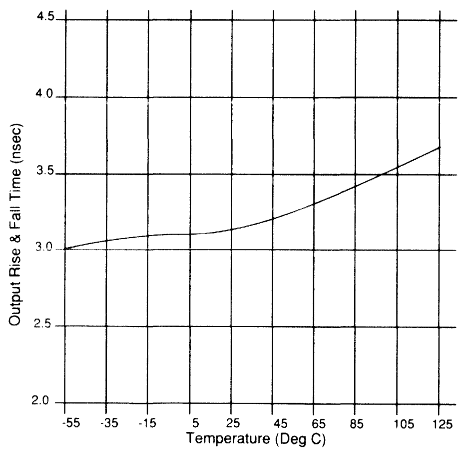
ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes.	Yes-shows up as elevated noise floor.	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts.	Yes-shows up as elevated noise floor.	Yes-part of RMS error	YES
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform).	Yes-shows up as harmonics of fundamental aliased into baseband.	Yes-part of RMS error	Yes
AAperature Uncertainty	No-averaged out. Can be measured with "phase locked" histrogram.	Yes-shows up as elevated noise floor.	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

CHARACTERIZATION GRAPHS



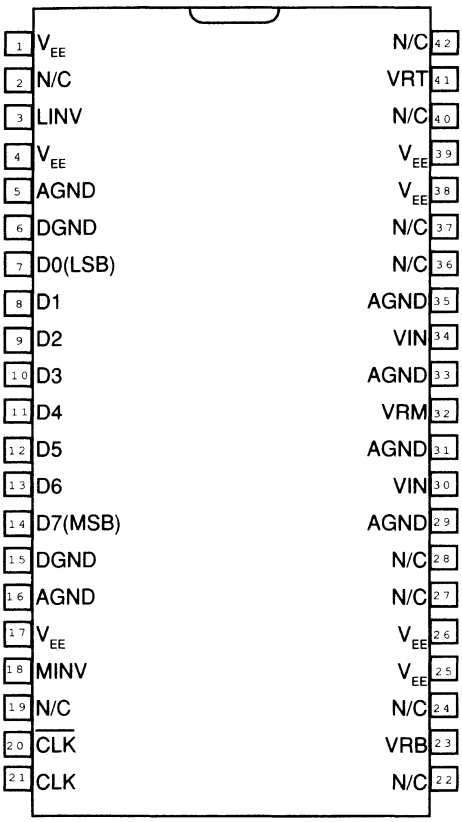






PIN ASSIGNMENT HADC77100

TOP VIEW



PIN FUNCTIONS HADC77100

NAME	FUNCTION
V_{EE}	Negative Supply Nominally -5.2 V
LINV	D0 through D6 Output Inversion Control Pin
DGND	Digital Ground
D0	Digital Data Output (LSB)
D1~D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control
CLK	ECL Clock Input Pin
$\overline{CLK}$	ECL Clock Input Pin
VRB	Reference Voltage Bottom Nominally -2.0 V
AGND	Analog Ground
VIN	Analog Input Can be connected to the input signal or used as Sense
VRM	Reference Voltage Tap Middle
VRT	Reference Voltage, Top Nominally 0.0 V

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3

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

HADC77200

8-BIT, 150 MSPS FLASH A/D CONVERTER

FEATURES

- 150 MSPS CONVERSION RATE
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Typical Power Dissipation < 2.2 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Medical Electronics: Ultrasound, CAT Instrumentation

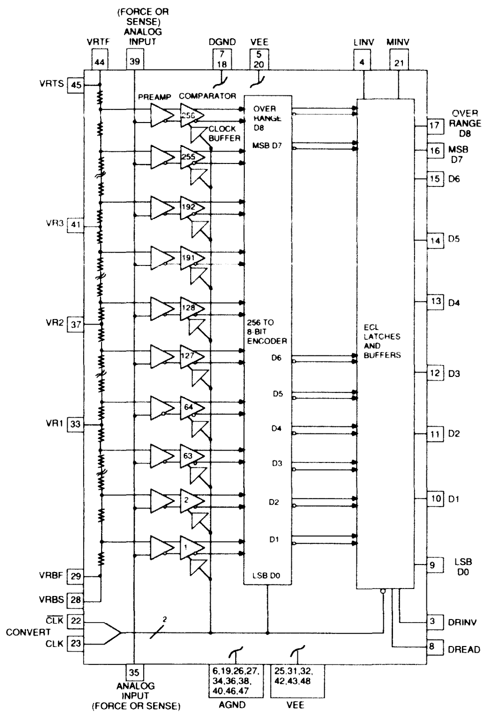
GENERAL DESCRIPTION

The HADC77200 is a monolithic flash A/D converter capable of digitizing a 2 volt analog input signal with full scale frequency components to 50 MHz into 8-bit digital words at a 150 MSPS (TYP) update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth. A single standard -5.2 volt power supply is required for operation of HADC77200, with nominal power dissipation of 2.2 watts.

The part is packaged in a 48 lead ceramic sidebrazed DIP. The HADC77200 includes five external reference ladder TAPS to gain better control over linearity; an overrange bit for use in higher resolution systems; and a data ready output pin for ease in interfacing to high-speed memory. Careful attention to design and layout has provided a device with a low noise floor, stable input characteristics, and low data error rate. The HADC77200 is available in industrial and military temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Negative Supply Voltage (V_{EE} TO GND)...............-7.0 to +0.5 V
Ground Voltage Differential..................................-0.5 to +0.5V

Input Voltage

Analog Input Voltage... +0.5V to V_{EE}
Reference Input Voltage..................................... +0.5V to V_{EE}
Digital Input Voltage.. +0.5V to V_{EE}
Reference Current VRT to VRB.................................. 25 mA
Tap Reference Current... -6 to +6 mA

Output

Digital Output Current... 0 to -25 mA

Temperature

Operating Temperature, ambient.........................-65 to +105 °C
case.......................................+125 °C
junction..................................+150 °C
Lead Temperature, (soldering 10 seconds)...................+300 °C
Storage Temperature..-65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_C=T_{CASE}=+125 °C, T_A=$T_{AMBIENT}$, V_{EE}=-5.2 V, R_{Source} =10 Ω, VRB=-2.00 V, VRT=0.00 V, f_{clk}=100 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25 °C MIN	TYP	MAX	HOT T_{MAX} MIN	MAX	COLD T_{MIN} MIN	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS										
Integral Linearity, 77200A	T_A = -25 to +85 °C	II			±1/2		±1/2		±1/2	LSB
	T_A = -55 to T_C	I			±1/2		±3/4		±3/4	LSB
Differential Linearity, 77200A (No missing codes)	T_A = -25 to +85 °C	II			±1/2		±1/2		±1/2	LSB
	T_A = -55 to T_C	I			±1/2		±3/4		±3/4	LSB
Integral Linearity, 77200B		II			±3/4		±3/4		±3/4	LSB
Differential Linearity, 77200B (No missing codes)		II			±3/4		±3/4		±3/4	LSB
Offset Error VRT	T_A = -25 to +85 °C	II			±30		±30		±30	mV
	T_A = -55 to T_C	I			±30		±30		±30	mV
Offset Error VRB	T_A = -25 to +85 °C	II			±30		±30		±30	mV
	T_A = -55 to T_C	I			±30		±30		±30	mV
Input Voltage Range	T_A = -25 to +85 °C	II	-2.0		0.0	-2.0	0.0	-2.0	0.0	Volts
	T_A = -55 to T_C	I	-2.0		0.0	-2.0	0.0	-2.0	0.0	Volts
Input Capacitance	Over full input range	V		45						pF
Input Resistance		V		100						kΩ
Input Current	T_A = -25 to +85 °C	II		300	500		450		650	µA
	T_A = -55 to T_C	I		300	500		400		750	µA
Clock Synchronous Input Currents		V		40						µA
Supply Current	T_A = -25 to +85 °C	II		420	505		525		505	mA
	T_A = -55 to T_C	I		420	505		535		505	mA
Power Dissipation		II		2.18	2.63		2.73		2.63	mA
Ladder Resistance	T_A = -25 to +85 °C	II	100		300	100	300	80	300	Ω
	T_A = -55 to T_C	I	100		300	130	300	60	300	Ω
Reference Bandwidth		V		50						MHz

ELECTRICAL SPECIFICATIONS

T_C=T_{CASE}=+125 °C, T_A=$T_{AMBIENT}$, V_{EE}=-5.2 V, R_{Source} =10 Ω, VRB=-2.00 V, VRT=0.00 V, f_{clk}=100 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	LEVEL	ROOM +25 °C MIN	ROOM +25 °C TYP	ROOM +25 °C MAX	HOT T_{MAX} MIN	HOT T_{MAX} MAX	COLD T_{MIN} MIN	COLD T_{MIN} MAX	UNITS
DIGITAL CHARACTERISTICS										
Output High Voltage	50 Ω to -2 V									
	T_A = -25 to +85 °C	II	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	Volts
	T_A = -55 to T_C	I	-0.98	-0.90	-0.82	-0.85	-0.66	-1.10	-0.95	Volts
Output Low Voltage	50 Ω to -2 V									
	T_A = -25 to +85 °C	II	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	Volts
	T_A = -55 to T_C	I	-1.95	-1.80	-1.65	-1.95	-1.65	-2.00	-1.70	Volts
Input High Voltage (MINV, LINV)	T_A = -25 to +85 °C	II	-1.13		-0.81	-1.07	-0.67	-1.19	-0.87	Volts
	T_A = -55 to T_C	I	-1.13		-0.81	-1.07	-0.67	-1.22	-0.87	Volts
Input Low Voltage (MINV, LINV)	T_A = -25 to +85 °C	II	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	Volts
	T_A = -55 to T_C	I	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	Volts
AC ELECTRICAL CHARACTERISTICS										
Maximum Sample Rate	T_A = -25 to +85 °C	IV	125	150		125		125		MSPS
	T_A = -55 to T_C	I	100	150		100		100		MSPS
Clock Low Width, TPW0	T_A = -25 to +85 °C	I	5	3						ns
	T_A = -55 to T_C	I	5	3		5		5		ns
Clock High Width, TPW1	T_A = -25 to +85 °C	I	5	3						ns
	T_A = -55 to T_C	I	5	3		5		5		ns
Output Delay, TD	T_A = -25 to +85 °C	I	3	4.2	5					ns
Differential Clock	T_A = -55 to T_C	I	3	4.2	5	4	7	3	4.5	ns
Output Delay Tempco Differential Clock		V		15						ps/°C
Data Ready Delay	T_A = -25 to +85 °C	I	3	4						ns
Differential Clock	T_A = -55 to T_C	I	3	4	5	3.8	7	3.5	4.5	ns
Output Rise Time 10 to 90%	T_A = -25 to +85 °C	I	1.3	1.9	2.4					ns
50 Ω to -2 V	T_A = -55 to T_C	I	1.3	1.9	2.4	1.3	4	.5	2.2	ns
Output Fall Time 10 to 90%	T_A = -25 to +85 °C	I	1.1	1.5	2.2					ns
50 Ω to -2 V	T_A = -55 to T_C	I	1.1	1.5	2.2	1.1	4	.5	2.2	ns
Large Signal Bandwidth	Vin = F.S.	V		100						MHz
Small Signal Bandwidth	Vin=500 mV PP	V		175						MHz
Aperture Jitter		V		12						ps
Aperture Delay	Differential Clock									
	T_A = -25 to +85 °C	I	0.3	1.8	2.3					ns
	T_A = -55 to T_C	I	0.3	1.8	2.3	0.3	2.8	0.3	2.0	ns
Aperture Delay Tempco	Differential Clock	V		4						ps/°C
Aperture Time		V		<100						ps
Acquisition Time	F.S. to ±1/2 LSB	V		5						ns
Input Slew Rate		V		800						V/µs

ELECTRICAL SPECIFICATIONS

T_C=T_{CASE}=+125 °C, T_A=$T_{AMBIENT}$, V_{EE}=-5.2 V, R_{Source} =10 Ω, VRB=-2.00 V, VRT=0.00 V, f_{clk}=100 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25 °C MIN	TYP	MAX	HOT T_{MAX} MIN	MAX	COLD T_{MIN} MIN	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS										
Total Dynamic Error	V_{in} = FS @ 1 MHz									
	T_A = -25 to +85 °C	I	45	48						dB
	T_A = -55 to T_C	I	45	48		44.2		44.2		dB
Total Dynamic Error	V_{in} = FS @ 25 MHz									
	T_A = -25 to +85 °C	I	36.7	38						dB
	T_A = -55 to T_C	I	36.7	38		36.2		36.2		dB
Total Dynamic Error, 77200A	V_{in} = FS @ 50 MHz									
	T_A = -25 to +85 °C	I	29.5	33						dB
	T_A = -55 to T_C	I	29.5	33		29.2		29.2		dB
Signal to Noise Ratio	V_{in} = FS @ 1 MHz									
	T_A = -25 to +85 °C	I	46.5	49						dB
	T_A = -55 to T_C	I	46.5	49		45		45		dB
Signal to Noise Ratio	V_{in} = FS @ 25 MHz									
	T_A = -25 to +85 °C	I	42.5	46						dB
	T_A = -55 to T_C	I	42.5	46		41		41		dB
Signal to Noise Ratio, 77200A	V_{in} = FS @ 50 MHz									
	T_A = -25 to +85 °C	I	33	38						dB
	T_A = -55 to T_C	I	33	38		32.5		32.5		dB
Total Harmonic Distortion	V_{in} = FS @ 1 MHz									
	T_A = -25 to +85 °C	I	52	56						dB
	T_A = -55 to T_C	I	52	56		50.5		52		dB
Total Harmonic Distortion	V_{in} = FS @ 25 MHz									
	T_A = -25 to +85 °C	I	38	39						dB
	T_A = -55 to T_C	I	38	39		36.5		38		dB
Total Harmonic Dist, 77200A	V_{in} = FS @ 50 MHz									
	T_A = -25 to +85 °C	I	32	34						dB
	T_A = -55 to T_C	I	32	34		30.5		32		dB

TEST LEVEL CODES

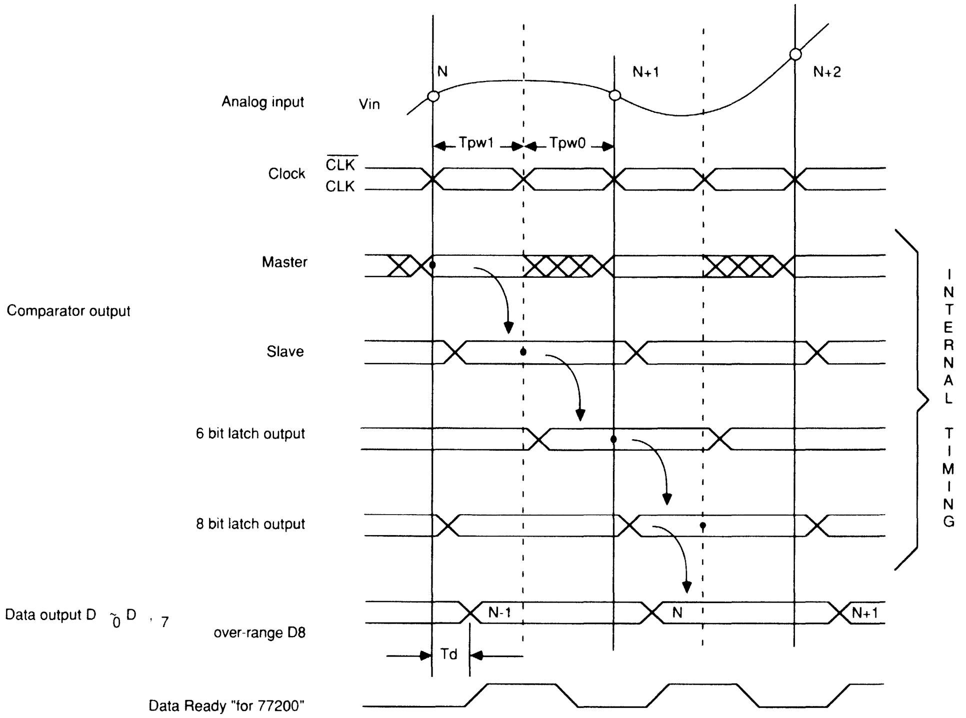
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are performed after die reaches operating temperature.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Timing Diagram



Dots (•) in the chart denote respective latch timings.

DEFINITION OF TERMS

A/D CONVERTER ERROR SUMMARY

SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 1B) while a static DC input level may appear close to the ideal (Figure 1A). That is why we are including many dynamic tests as well as the industry standard DC specifications.

TOTAL DYNAMIC ERROR (EFFECTIVE BITS)

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These errors are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from the measured RMS error for the ideal sinewave and the measured actual RMS error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual RMS error}}{\text{ideal RMS error}}$$

Furthermore, total dynamic error (TDE) can be related to effective bits by the following formula:

$$\text{TDE (dB)} = 1.8 + 6.02 \text{ X N (eff bits)}$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = FSR/2^N$ where FSR = full scale range and N = 8. Nonideal quantization bands represent differential nonlinearity errors see Figures 1A and 1B.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 1B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77200's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 1B points out two missed codes in the transfer function.

Figure 1A - Static Input Conditions

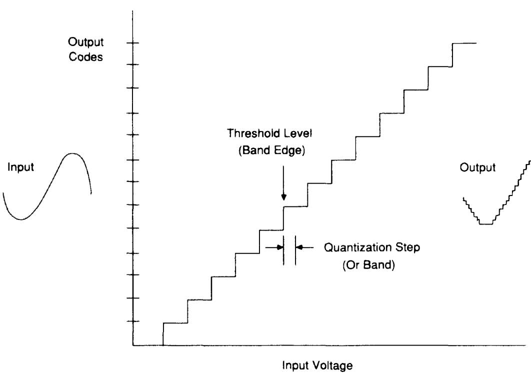
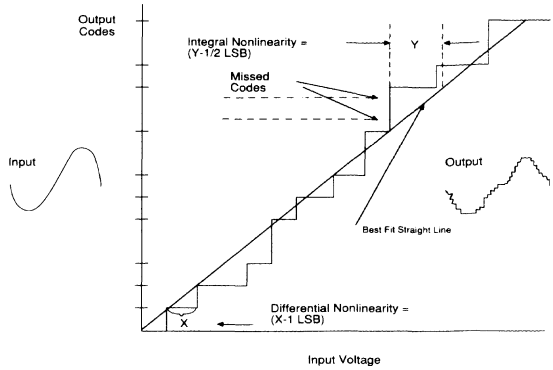


Figure 1B - Dynamic Conditions



INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 2A). Integral nonlinearity does not include any gain or offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 1B shows an integral nonlinearity error of 2 LSBs. The HADC77200's integral nonlinearity can be improved by using the external reference ladder taps as shown in Figure 5. The resulting effect on the linearity is shown in Figure 2B.

Figure 2A - Linearity Curve with no TAP adjustment

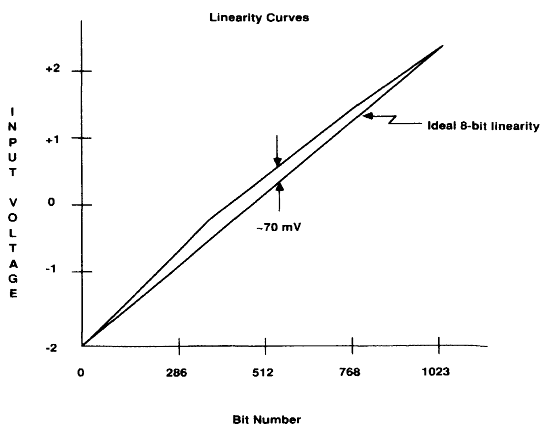
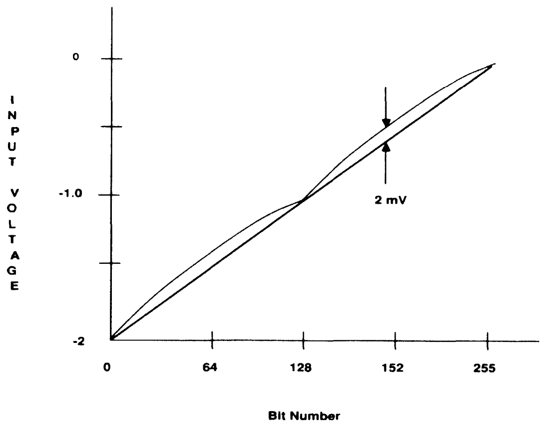


Figure 2B - Linearity Curve with TAP Forced to Within .5 mV of Ideal



APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point see Figure 2C.

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sinewave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi f t_A$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 3 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal frequencies.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10 MHz, then from Figure 3 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70 ps. Most data sheets do not state aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70 ps.

Aperture time and delay are very difficult to measure. However, these values are needed to make intelligent design decisions. SPT supplies these values for the HADC77200 based on both computer design simulations and verified by characterization of samples.

Figure 2C - Aperture Uncertainty

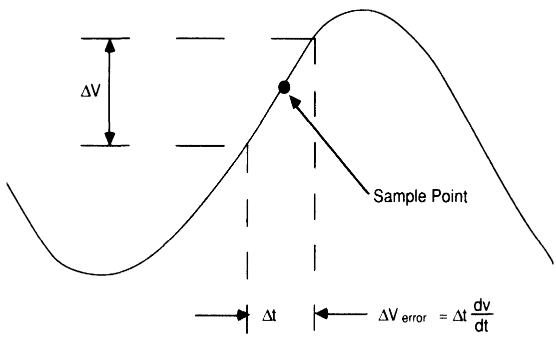
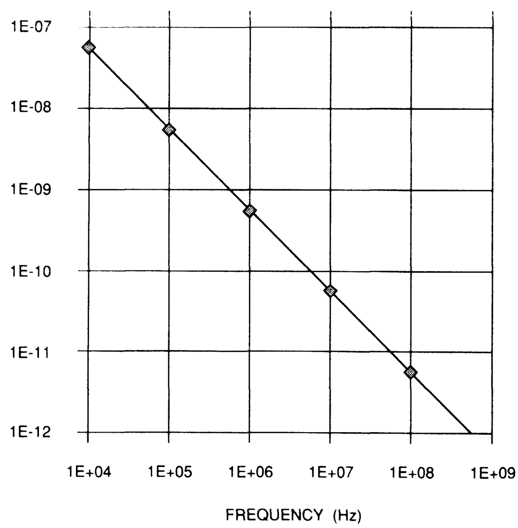


Figure 3 - Aperture Time - Sinewaves



$$t_A = \frac{1}{2^N \, 2\pi f}$$

$N = 8$

CHARACTERISTIC TESTING

TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table I.

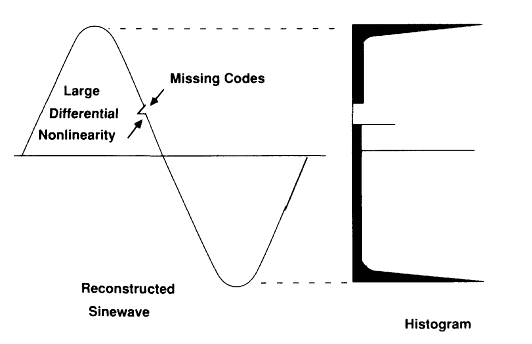
HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77200. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurrence along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{-1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurrence at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts see Figure 4.

Figure 4 - Histogram Testing



In the histogram test, the A/D transfer function step widths larger than ideal show up as "spikes" in the histogram. Codes missing from the transfer function show up as "bins" with zero counts.

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sinewave, caused by the integral nonlinearity, are aliased into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table I.

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77200. Using least squared error minimization techniques, an idealized sinewave fit to the data is calculated by software. The sinewave is in the form:

$$A\sin(2\pi ft+\theta)+DC$$

where A, f, θ, DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave,

$$A_0\sin(2\pi f_0t+\theta_0)+DC_0$$

is then subtracted from the digitized time record. The rms errors are then calculated and the effective bits specification is found.

BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77200. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converters sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δ f, is observed. Differential nonlinearities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

DYNAMIC EVALUATION

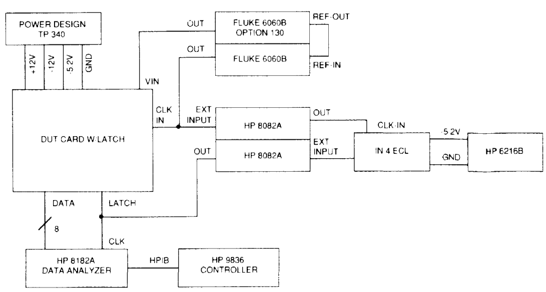


Table I - Tests

The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

(Table from H.P. Product Note 5180A-2)

ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes.	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts.	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform).	Yes-shows up as harmonics of fundamental aliased into baseband	Yes-part of RMS error	Yes
Aperture Uncertainty	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

GENERAL DESCRIPTION

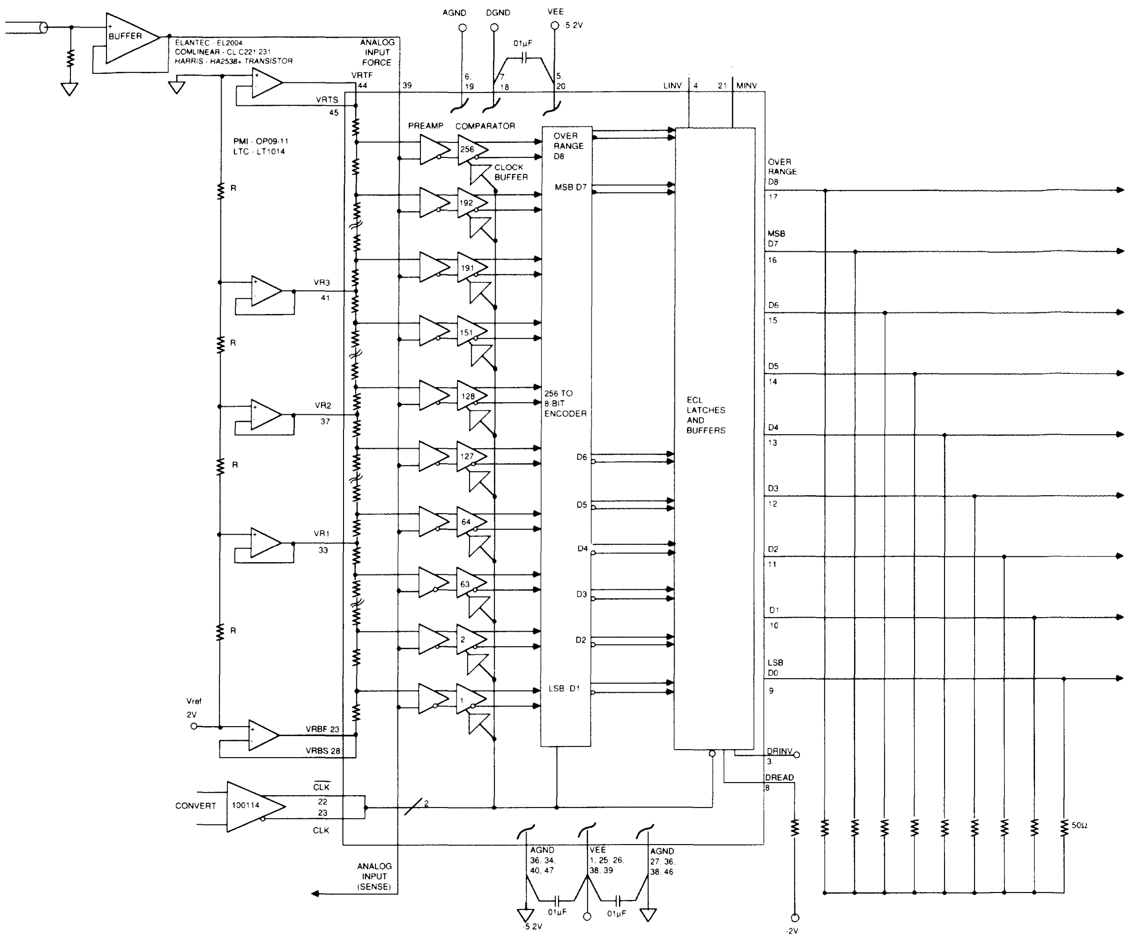
The HADC77200 is the fastest monolithic 8-bit parallel flash A/D converter available today. The minimum conversion rate is 150 MSPS and the analog bandwidth is in excess of 100 MHz. A major advance over previous flash converters is the enclosed 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This reduces clock transient kickback to the input and reference ladder. The preamplifiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range of "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

An additional advantage of the HADC77200 over similar devices is a better integral linearity specification over the parts entire usable range. The center reference ladder taps are optional as needed to further improve this specification.

The HADC77200 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77200 has an on board power supply bypass of 1500 pF to reduce external component needs. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

FIGURE 5 - HADC77200 Typical Interface Circuit



TYPICAL INTERFACE CIRCUIT

The HADC77200 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 5 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 5.

VIN (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force." This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77200 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836 transistor. Very high performance can be achieved by using a Comlinear CLC221/231.

CLK, $\overline{\text{CLK}}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{\text{CLK}}$ is internally biased to -1.3 V. (See clock input circuit.) It may be left open but a .01µF bypass capacitor from $\overline{\text{CLK}}$ to AGND is recommended. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

MINV, LINV (OUTPUT LOGIC CONTROL)

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table II. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to AGND1 through a diode or 3.9 kΩ resistor.

D0 TO D7 (DIGITAL OUTPUTS)

The digital outputs can drive 50 Ω to ECL levels when pulled down to -2V. When pulled down to -5.2 V the outputs can drive 130 Ω to 1 kΩ loads.

Table II - Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS (REFERENCE INPUTS)

These are five external reference voltage taps from -2V (VRB) to AGND (VRT) which can be used to control integral linearity over temperature. The taps can be driven by op amps as shown in Figure 5. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired. VRB and VRT have "force" and "sense" pins for monitoring the top and bottom voltage references.

DREAD (DATA READY), DRINV (DATA READY INVERSE)

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the HADC77200's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin (see Timing Diagram).

D8 (Overrange)

This is an overrange function. When the HADC77200 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the HADC77200 into higher resolution systems.

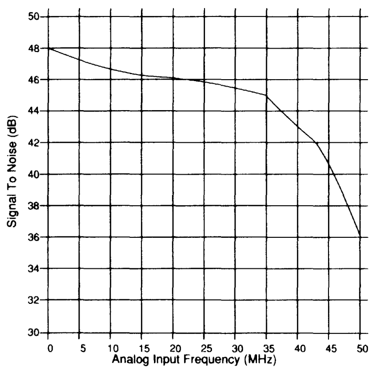
N/C

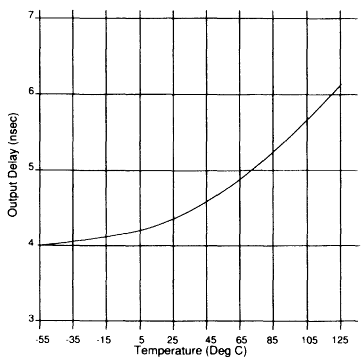
All "Not Connected" pins should be tied to AGND.

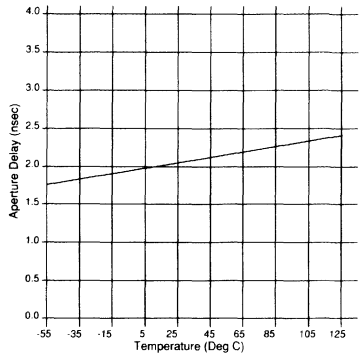
OPERATION

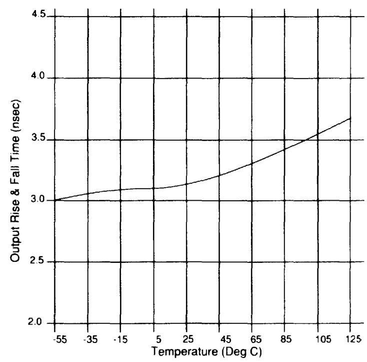
The HADC77200 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

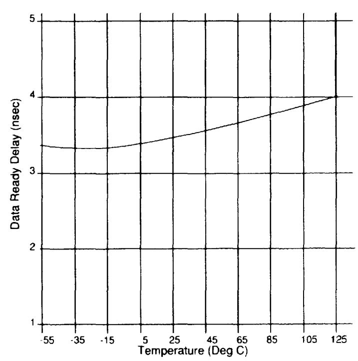
CHARACTERIZATION GRAPHS





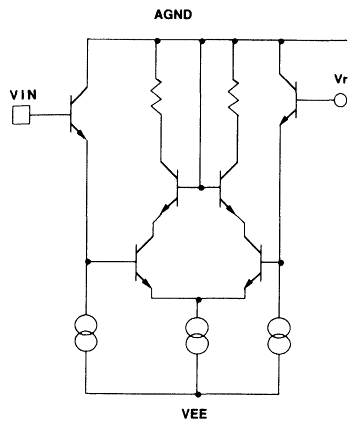




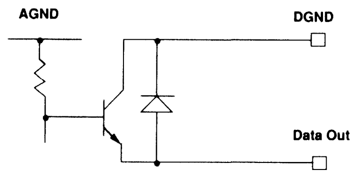


SUBCIRCUIT SCHEMATICS

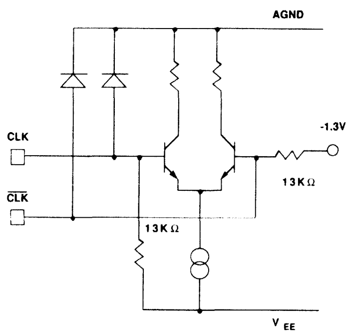
INPUT CIRCUIT



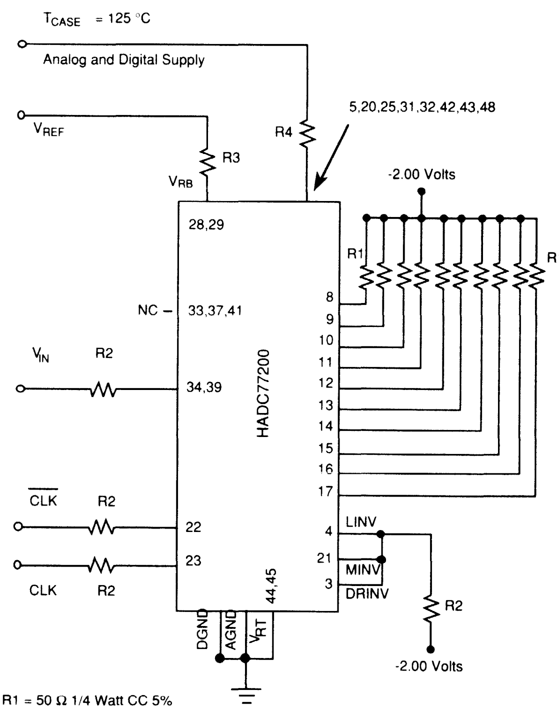
OUTPUT CIRCUIT



CLOCK INPUT

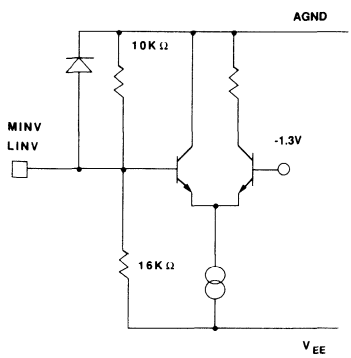


BURN-IN CIRCUIT



R1 = 50 Ω 1/4 Watt CC 5%
R2 = 1kΩ 1/4 Watt CC 5%
R3 = 6.5 Ω 1/4 Watt CC 5%
R4 = 3.25 Ω 1/2 Watt CC 5%
V_{REF} = -2.00 Volts
VEE = -6.6 Volts

DRINV, MINV, LINV INPUT CIRCUIT



PIN ASSIGNMENT HADC77200

TOP VIEW

1	N/C	VEE	48
2	N/C	AGND	47
3	DRINV	AGND	46
4	LINV	VRTS	45
5	VEE	VRTF	44
6	AGND	VEE	43
7	DGND	VEE	42
8	DREAD	VR3	41
9	D0 (LSB)	AGND	40
10	D1	VIN	39
11	D2	AGND	38
12	D3	VR2	37
13	D4	AGND	36
14	D5	VIN	35
15	D6	AGND	34
16	D7 (MSB)	VR1	33
17	D8 (OVERRANGE)	VEE	32
18	DGND	VEE	31
19	AGND	N/C	30
20	VEE	VRBF	29
21	MINV	VRBS	28
22	$\overline{\text{CLK}}$	AGND	27
23	CLK	AGND	26
24	N/C	VEE	25

PIN FUNCTIONS HADC77200

NAME	FUNCTION
VEE	Negative Supply Nominally -5.2 V
LINV	D0 through D6 Output Inversion Control Pin
DREAD	Data Ready Output
DGND	Digital Ground
AGND	Analog Ground
D0	Digital Data Output Pin 1 (LSB)
D1-D6	Digital Data Output Pin 7
D8	Overrange Output
MINV	D7 Output Inversion Control Pin
CLK	ECL Clock Input Pin
$\overline{\text{CLK}}$	ECL Clock Input Pin
DRINV	Data Ready Inverse
VRBS	Reference Voltage Bottom, Sense Nominally -2.0 V
VRBF	Reference Voltage Bottom, Force, Nominally-2.0 V
VIN	Analog Input, connected to the input signal or used as Sense
VR1	Reference Voltage Tap 1
VR2	Reference Voltage Tap 2
VR3	Reference Voltage Tap 3
VRTS	Reference Voltage Top, Sense, Nominally -2.0 V
VRTS	Reference Voltage Top, Force, Nominally -2.0 V

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3

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

SPT7810

10-BIT, 20 MHz A/D CONVERTER

PRELIMINARY INFORMATION

3

FEATURES

- Monolithic 20 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 57 dB SNR @ 3.58 MHz Input
- Low Power (1.3 W Typical)
- 5 pF input Capacitance
- ECL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

GENERAL DESCRIPTION

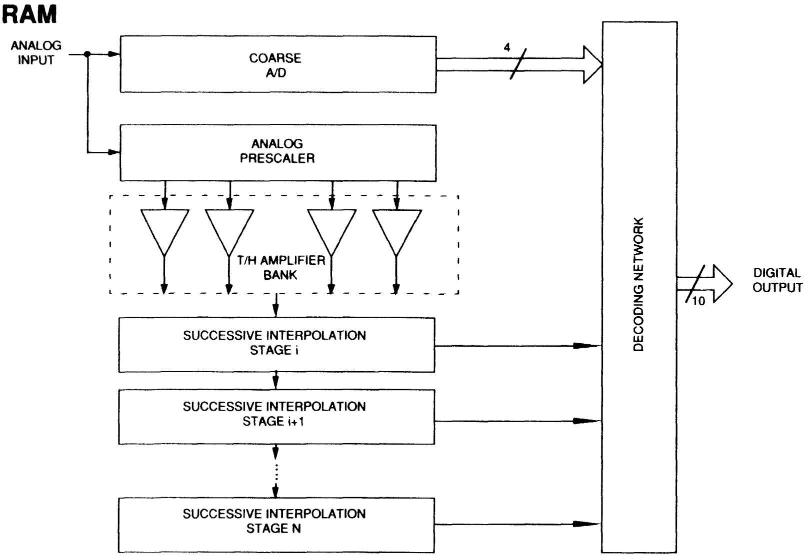
The SPT7810 A/D converter is a 10-bit monolithic converter capable of word rates of up to 30 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions.

Output data format is straight binary. Power dissipation is very low at only 1.3 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7810 also provides a wide input voltage swing of ±2.0 volts.

The SPT7810 is available in a small 28-lead ceramic sidebrazed DIP package and in die form. An industrial temperature range of -25 to +85 °C is currently offered with military temperature and /883 processed units to be available in the near future.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
V_{CC} .... +6 V
V_{EE} .... -6 V

Input Voltages
Analog Input .... $\leq V_{FT}$, $\geq V_{FB}$
V_{FT}, V_{FB} .... +3.0 V, -3.0 V
Reference Ladder Current .... 12 mA

Output
Digital Outputs .... 0 to -30 mA

Temperature
Operating Temperature .... -65 to +150 °C
Junction Temperature .... 175 °C
Lead Temperature, (soldering 10 seconds) .... 300 °C
Storage Temperature .... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{FB}=-2.5 V, V_{FT}=+2.5 V, f_{clock}=20 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7810A MIN	SPT7810A TYP	SPT7810A MAX	SPT7810B MIN	SPT7810B TYP	SPT7810B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy									
Integral Nonlinearity		II		±1.0			±1.5		LSB
Differential Nonlinearity		II		±0.5			±0.75		LSB
No Missing Codes				Guaranteed					
Analog Input									
Input Voltage Range		II		±2.0			±2.0		V
Input Bias Current		II		30	40		30	40	µA
Input Resistance	V_{IN}=0 V	II		300			300		KΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error				±2.0			±2.0		LSB
-FS Error				±2.0			±2.0		LSB
Midscale Error				±0.5			±0.5		LSB
Reference Input									
Reference Ladder Resistance		II	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Reference Ladder Bandwidth		V		50			50		MHz
Conversion Characteristics									
Maximum Conversion Rate		II	20			20			MHz
Output Delay				4			4		ns
Acquisition Time				20			20		ns
Aperture Delay Time				1			1		ns
Aperture Jitter Time				5			5		ps-RMS

ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{FB}=-2.5 V, V_{FT}=+2.5 V, f_{clock}=20 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7810A MIN	SPT7810A TYP	SPT7810A MAX	SPT7810B MIN	SPT7810B TYP	SPT7810B MAX	UNITS
Dynamic Performance									
Effective Bits									
fin=1 MHz				9.0			8.5		Bits
fin=3.58 MHz				8.8			8.3		Bits
fin=10 MHz				7.5			7.0		Bits
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz		II	57	59		54	56		dB
fin=3.58 MHz		II	56	58		53	55		dB
fin=10 MHz		II	50	53		47	49		dB
Total Dynamic Error									
fin=1 MHz		II	55	56		52	53		dB
fin=3.58 MHz		II	54	55		51	52		dB
fin=10 MHz		II	44	47		41	44		dB
Harmonic Distortion									
fin=1 MHz	64 Distortion BINS from	II	57	59		54	56		dB
fin=3.58 MHz	4096 pt FFT	II	56	58		53	55		dB
fin=10 MHz		II	46	48		43	45		dB
Digital Inputs									
Logic "1" Voltage		V	-1.1			-1.1			V
Logic "0" Voltage		V			-1.5			-1.5	V
Maximum Input Current Low		II	-500	±200	+750	-500	±200	+750	µA
Maximum Input Current High		II	-500	±300	+750	-500	+300	+750	µA
Pulse Width Low (CLK)			20			20			ns
Pulse Width High (CLK)			20		300	20		300	ns
Digital Outputs									
Logic "1" Voltage	50 Ω to -2 V	II	-1.1	-0.8		-1.1	-0.8		V
Logic "0" Voltage	50 Ω to -2 V	II		-1.8	-1.5		-1.8	-1.5	V
Power Supply Requirements									
Voltages V_{CC}		IV	+4.5		+5.5	+4.5		+5.5	V
$-V_{EE}$		IV	-4.7		-5.7	-4.7		-5.7	V
Currents I_{CC}		II		140	170		140	190	mA
$-I_{EE}$		II		115	140		115	160	mA
Power Dissipation	Outputs Open	II		1.3	1.6		1.3	1.8	W
Power Supply Rejection Ratio				70			70		dB

Figure 1A: Timing Diagram

(N is the first rising edge of the CLK after the device is powered up)

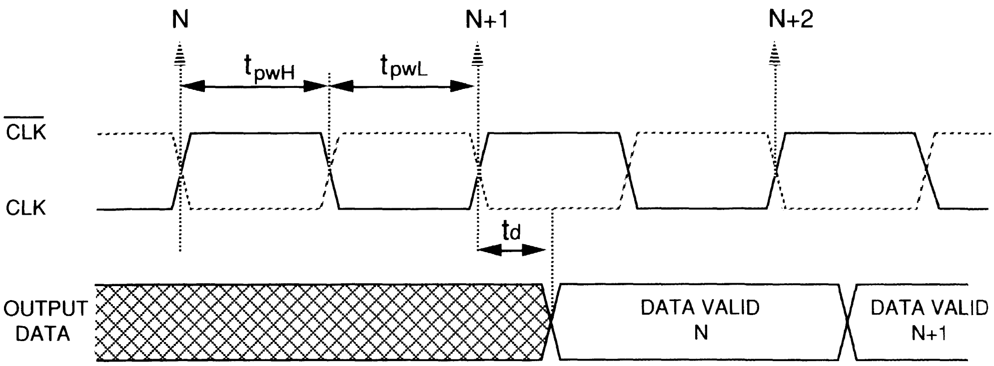
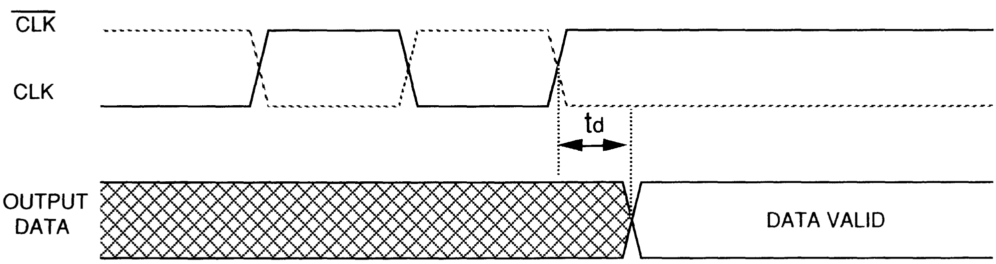


Figure 1B: Single Event Clock



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

TYPICAL INTERFACE CIRCUIT

The SPT7810 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7810 in normal circuit operation.
The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

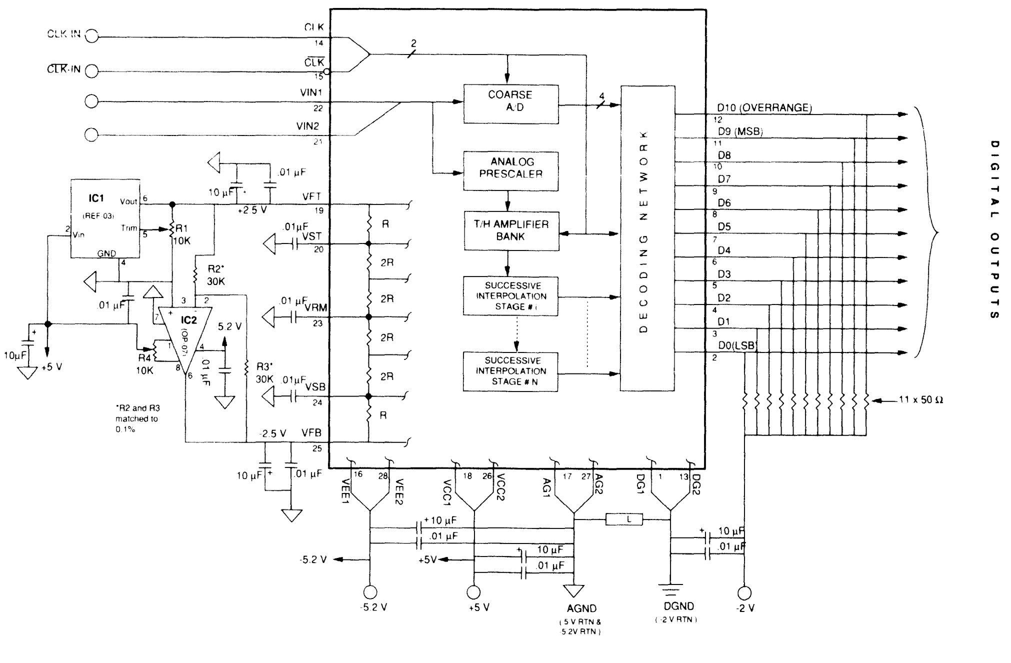
The SPT7810 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in Figure 2.

The two grounds available on the SPT7810 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7810. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7810 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are 3 reference ladder taps (V_{ST}, V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit



An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10k ohms and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:

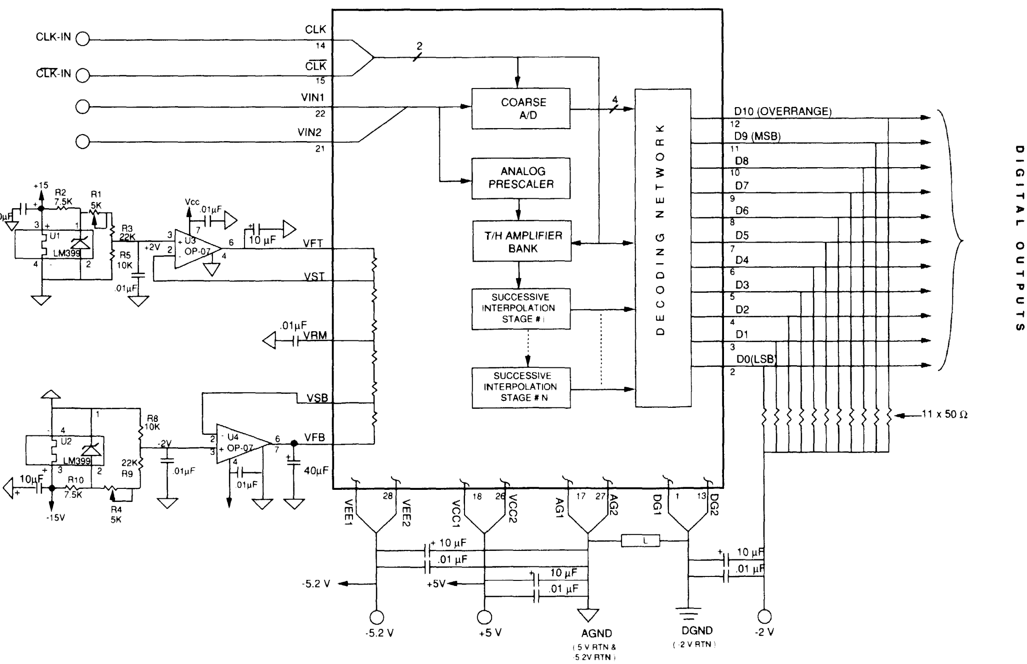
+FS error = top of ladder offset voltage = $\Delta(+FS - V_{ST})$
-FS error = bottom of ladder offset voltage = $\Delta(-FS - V_{SB})$

Where the +FS (full scale) input voltage is defined as the output approximately 1 mV above the transition of 1—10 and 1—11 and the -FS input voltage is defined as the output approximately 1 mV below the transition of 0—00 and 0—01.

An example of an alternate reference driver circuit is shown in figure 3. This circuit is to be used to minimize the +FS and -FS errors over temperature. U1 and U2 are LM339s with an output voltage of +2 V and -2 V respectively. U3 and U4 are recommended to be OP-07s or equivalent. The input offset of these devices is 150 uV maximum. This circuit uses a true force and sense when driving the reference ladder of the SPT7810. U3 sources the current through V_{FT} (V_{ST} is a sense) while U4 is sinking current through V_{FB} (V_{SB} is a sense). To calibrate the reference, adjust R1 for V_{ST}=+2.0 V (V_{FT} will be typically +2.5 V) and adjust R4 for V_{SB}=-2.0 V (V_{FB} will be typically -2.5 V). This circuit is preferred because it allows the user to know exactly what the full scale input voltage is.

Note: U3 and U4 are biased from the +5.0 V and -5.2 V supplies to prevent the absolute maximum ratings of V_{FT} and V_{FB} from being exceeded in the event of an open circuit on U3 or U4.

Figure 3 - Alternate Interface Circuit



SPT

ANALOG INPUT

V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7810's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

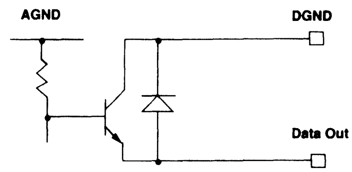
The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V. $\overline{CLK}$ may be left open, but a .01 μF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier (see timing diagram). The analog input signal is latched on the rising edge of the CLK.

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. These outputs are ECL with the output circuit shown in figure 4. The outputs are latched on the rising edge of CLK with a propagation delay of 4 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the capacitive loads in relation to the operating frequency must be considered.

Figure 4 - Output Circuit



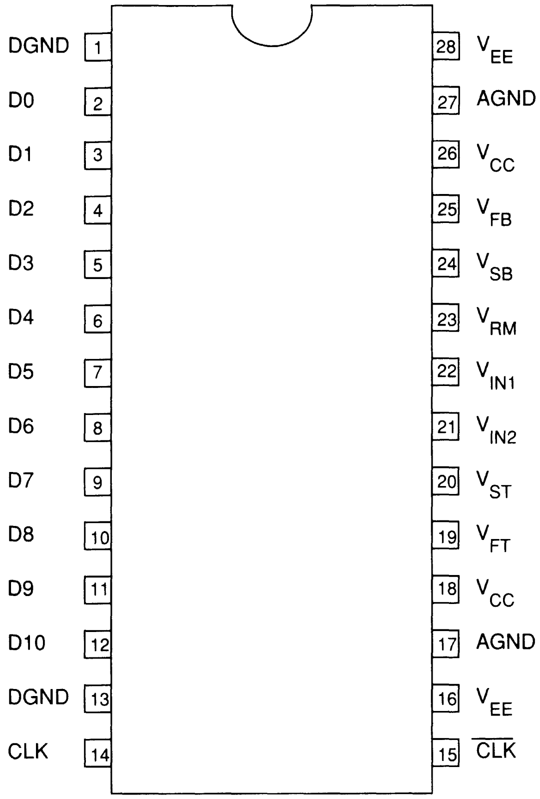
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the output will switch to logic 1. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7810 into higher resolution systems.

EVALUATION BOARD

The EB7810 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7810. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	ECL Outputs (D0=LSB)
D10	ECL Output Overrange
CLK	Clock
$\overline{CLK}$	Inverted Clock
V_{EE}	-5.2 V Supply
AGND	Analog Ground
V_{CC}	+5.0 V supply
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder
V_{RM}	Middle of Reference Ladder

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3

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

SPT7814

10-BIT, 40 MSPS A/D CONVERTER

PRELIMINARY INFORMATION

FEATURES

- Monolithic 40 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 55 dB SNR @ 3.58 MHz Input
- 50 dB SNR @ 10.3 MHz Input
- Low Power (1.3 W Typical)
- 5 pF input Capacitance
- ECL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

3

GENERAL DESCRIPTION

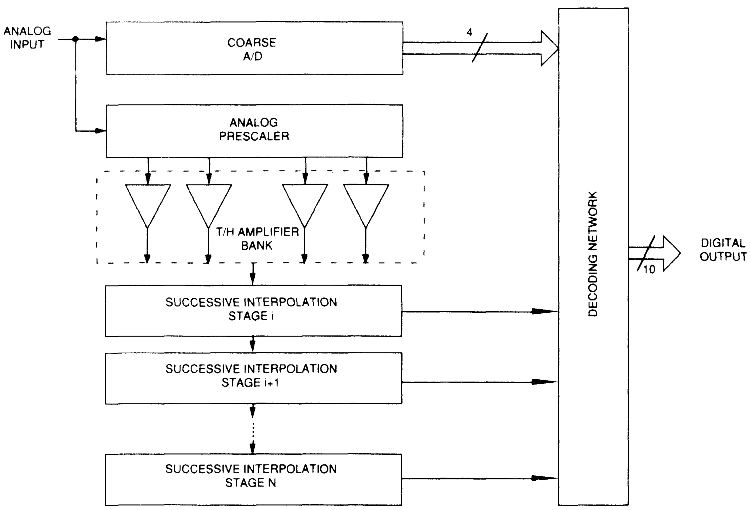
The SPT7814 A/D converter is a 10-bit monolithic converter capable of word rates of up to 50 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions.

Output data format is straight binary. Power dissipation is very low at only 1.3 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7814 also provides a wide input voltage swing of ±2.0 volts.

The SPT7814 is available in a small 28-lead ceramic sidebrazed DIP package, LCC, and die form. An industrial temperature range of -25 to +85 °C is currently offered with military temperature and /883 processed units to be available in the near future.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
V_{CC} .... +6 V
V_{EE} .... -6 V

Input Voltages
Analog Input .... $\leq V_{FT}$, $\geq V_{FB}$
V_{FT}, V_{FB}. .... +3.0 V, -3.0 V
Reference Ladder Current .... 12 mA

Output
Digital Outputs .... 0 to -30 mA

Temperature
Operating Temperature .... -65 to +150 °C
Junction Temperature .... 175 °C
Lead Temperature, (soldering 10 seconds) .... 300 °C
Storage Temperature .... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{FB}=-2.5 V, V_{FT}=+2.5 V, f_{clock}40 MHz, unless otherwise specified..

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7814A MIN	SPT7814A TYP	SPT7814A MAX	SPT7814B MIN	SPT7814B TYP	SPT7814B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy									
Integral Nonlinearity		II		±1.0			±1.5		LSB
Differential Nonlinearity		II		±0.5			±0.75		LSB
No Missing Codes				Guaranteed					
Analog Input									
Input Voltage Range		II		±2.0			±2.0		V
Input Bias Current		II		30	40		30	40	µA
Input Resistance	V_{IN}=0 V	II		300			300		KΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error				±2.0			±2.0		LSB
-FS Error				±2.0			±2.0		LSB
Midscale Error				±0.5			±0.5		LSB
Reference Input									
Reference Ladder Resistance		II	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Reference Ladder Bandwidth		V		50			50		MHz
Conversion Characteristics									
Maximum Conversion Rate		II	40			40			MHz
Output Delay				4			4		ns
Acquisition Time				20			20		ns
Aperture Delay Time				1			1		ns
Aperture Jitter Time				5			5		ps-RMS

ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{FB}=-2.5 V, V_{FT}=+2.5 V, f_{clock}=40 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7814A MIN	SPT7814A TYP	SPT7814A MAX	SPT7814B MIN	SPT7814B TYP	SPT7814B MAX	UNITS
Dynamic Performance									
Effective Bits									
fin=1 MHz				8.7			8.2		Bits
fin=3.58 MHz				8.7			8.2		Bits
fin=10.3 MHz				7.3			6.9		Bits
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz		II	55	57		52	54		dB
fin=3.58 MHz		II	55	57		52	54		dB
fin=10.3 MHz		II	48	50		46	48		dB
Harmonic Distortion									
fin=1 MHz	64 Distortion BINS from	II	54	56		52	54		dB
fin=3.58 MHz	4096 pt FFT	II	54	56		52	54		dB
fin=10.3 MHz		II	46	48		43	45		dB
Total Dynamic Error									
fin=1 MHz		II	52	54		49	51		dB
fin=3.58 MHz		II	52	54		49	51		dB
fin=10.3 MHz		II	44	46		41	43		dB
Digital Inputs									
Logic "1" Voltage		V	-1.1			-1.1			V
Logic "0" Voltage		V			-1.5			-1.5	V
Maximum Input Current Low		II	-500	±200	+750	-500	±200	+750	μA
Maximum Input Current High		II	-500	±300	+750	-500	+300	+750	μA
Pulse Width Low (CLK)			20			20			ns
Pulse Width High (CLK)			20		300	20		300	ns
Digital Outputs									
Logic "1" Voltage	50 Ω to -2 V	II	-1.1	-0.8		-1.1	-0.8		V
Logic "0" Voltage	50 Ω to -2 V	II		-1.8	-1.5		-1.8	-1.5	V
Power Supply Requirements									
Voltages V_{CC}		IV	+4.5		+5.5	+4.5		+5.5	V
$-V_{EE}$		IV	-4.7		-5.7	-4.7		-5.7	V
Currents I_{CC}		II		140	170		140	190	mA
$-I_{EE}$		II		115	140		115	160	mA
Power Dissipation	Outputs Open	II		1.3	1.6		1.3	1.8	W
Power Supply Rejection Ratio				70			70		dB

Figure 1A: Timing Diagram

(N is the first rising edge of the CLK after the device is powered up)

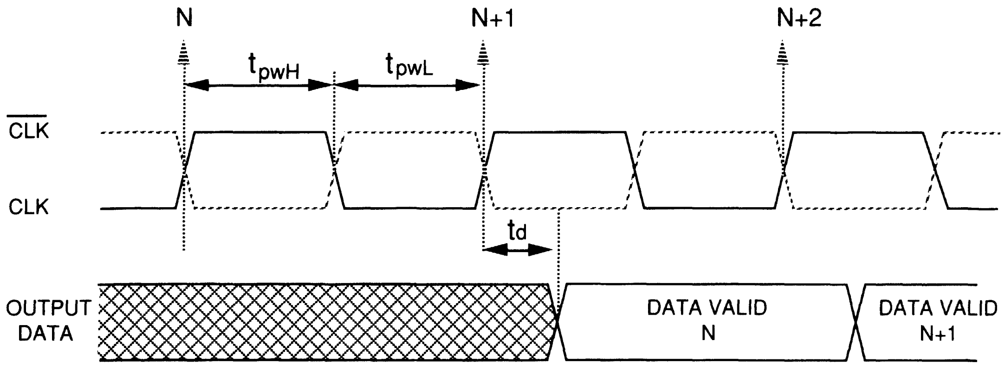
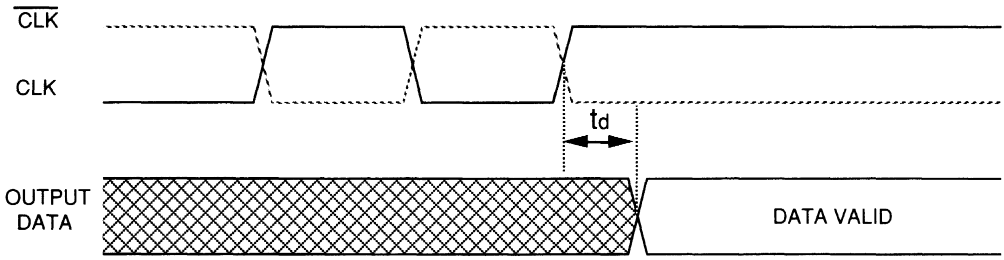


Figure 1B: Single Event Clock



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

TYPICAL INTERFACE CIRCUIT

The SPT7814 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7814 in normal circuit operation.
The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

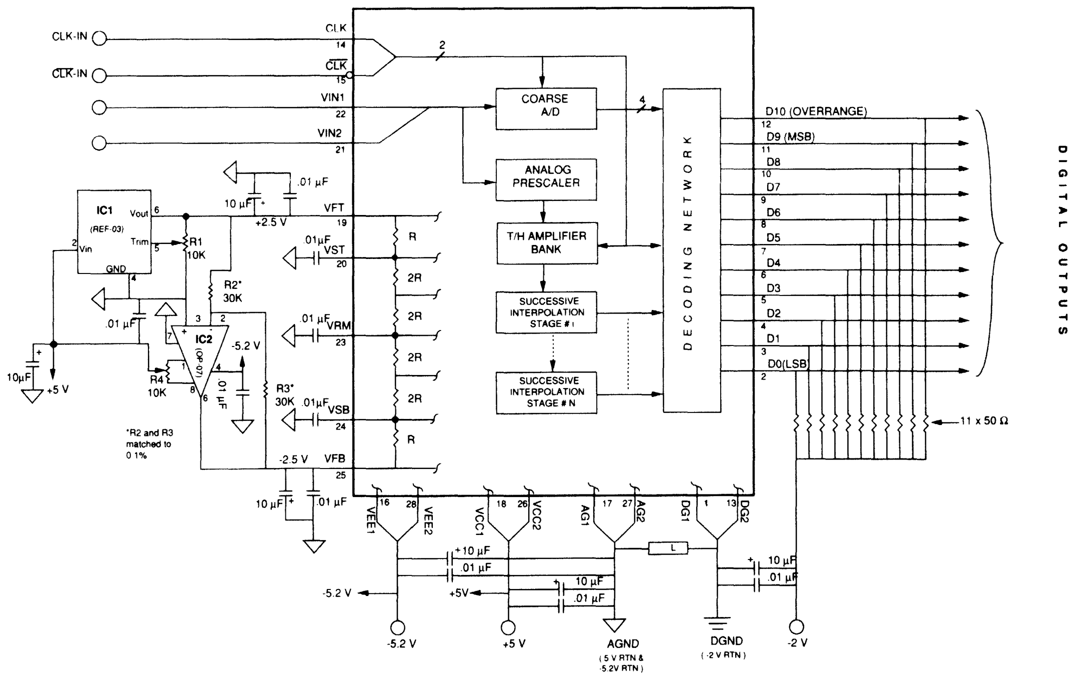
The SPT7814 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in Figure 2.

The two grounds available on the SPT7814 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7814. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7814 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are 3 reference ladder taps (V_{ST}, V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit



An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10k ohms and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:

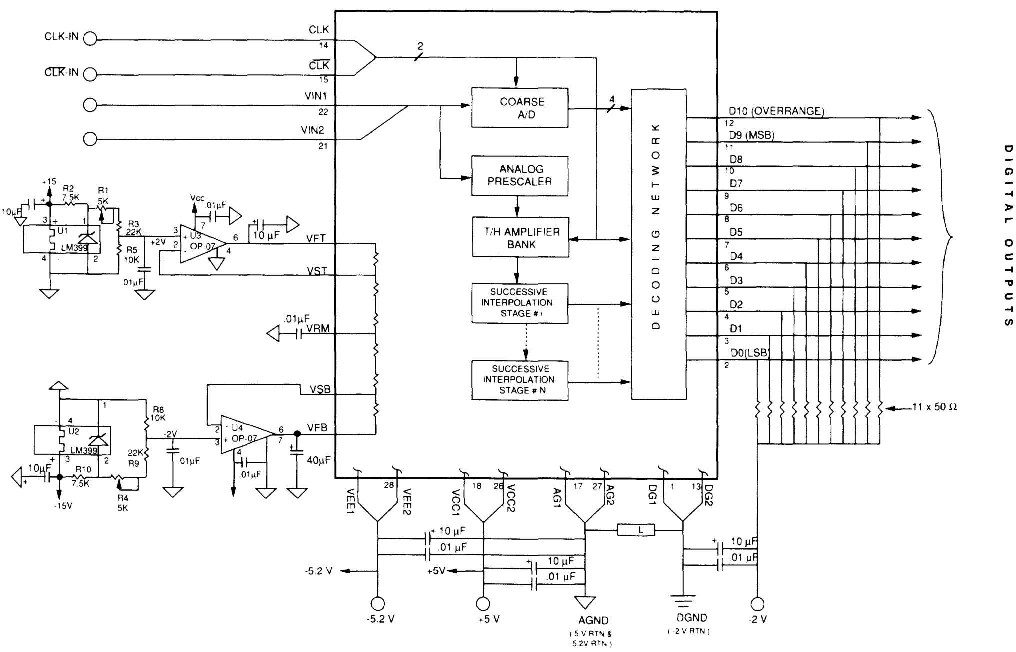
+FS error = top of ladder offset voltage = $\Delta(+FS - V_{ST})$
-FS error = bottom of ladder offset voltage = $\Delta(-FS - V_{SB})$

Where the +FS (full scale) input voltage is defined as the output approximately 1 mV above the transition of 1—10 and 1—11 and the -FS input voltage is defined as the output approximately 1 mV below the transition of 0—00 and 0—01.

An example of an alternate reference driver circuit is shown in figure 3. This circuit is to be used to minimize the +FS and -FS errors over temperature. U1 and U2 are LM339s with an output voltage of +2 V and -2 V respectively. U3 and U4 are recommended to be OP-07s or equivalent. The input offset of these devices is 150 uV maximum. This circuit uses a true force and sense when driving the reference ladder of the SPT7814. U3 sources the current through V_{FT} (V_{ST} is a sense) while U4 is sinking current through V_{FB} (V_{SB} is a sense). To calibrate the reference, adjust R1 for V_{ST}=+2.0 V (V_{FT} will be typically +2.5 V) and adjust R4 for V_{SB}=-2.0 V (V_{FB} will be typically -2.5 V). This circuit is preferred because it allows the user to know exactly what the full scale input voltage is.

Note: U3 and U4 are biased from the +5.0 V and -5.2 V supplies to prevent the absolute maximum ratings of V_{FT} and V_{FB} from being exceeded in the event of an open circuit on U3 or U4.

Figure 3 - Alternate Interface Circuit



ANALOG INPUT

V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7810's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

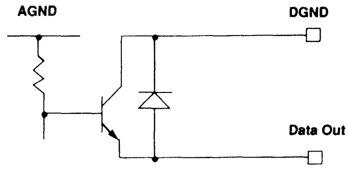
The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V. $\overline{CLK}$ may be left open, but a .01 μF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier (see timing diagram). The analog input signal is latched on the rising edge of the CLK.

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. These outputs are ECL with the output circuit shown in Figure 4. The outputs are latched on the rising edge of CLK with a propagation delay of 4 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the capacitive loads in relation to the operating frequency must be considered.

Figure 4 - Output Circuit



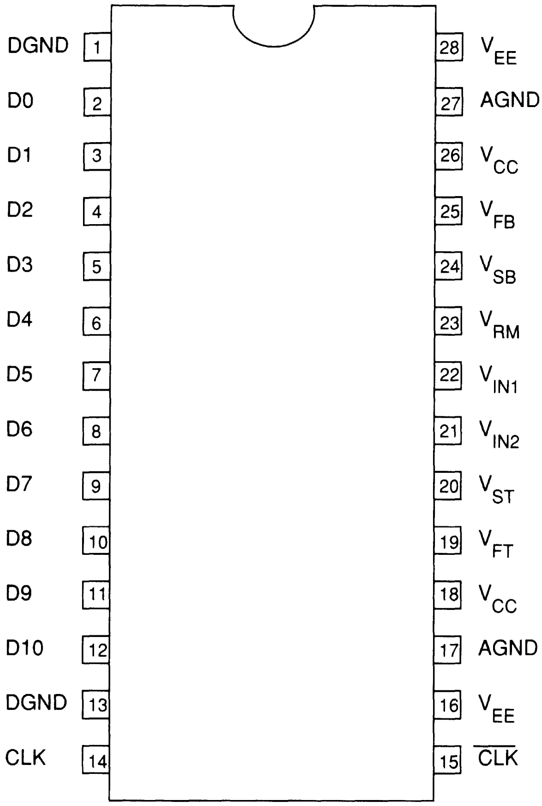
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the output will switch to logic 1. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7814 into higher resolution systems.

EVALUATION BOARD

The EB7814 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7814. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7814 is also available. Contact the factory for price and availability.

PIN ASSIGNMENT



PIN FUNCTIONS

NNAME	FUNCTION
DGND	Digital Ground
D0-D9	ECL Outputs (D0=LSB)
D10	ECL Output Overrange
CLK	Clock
$\overline{CLK}$	Inverted Clock
V_{EE}	-5.2 V Supply
AGND	Analog Ground
V_{CC}	+5.0 V supply
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder
V_{RM}	Middle of Reference Ladder

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3

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

SPT7820

10-BIT, 20 MHz, TTL, A/D CONVERTER

ADVANCE INFORMATION

FEATURES

- Monolithic 20 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 58 dB SNR @ 3.58 MHz Input
- Low Power (1.0 W Typical)
- 5 pF input Capacitance
- TTL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

3

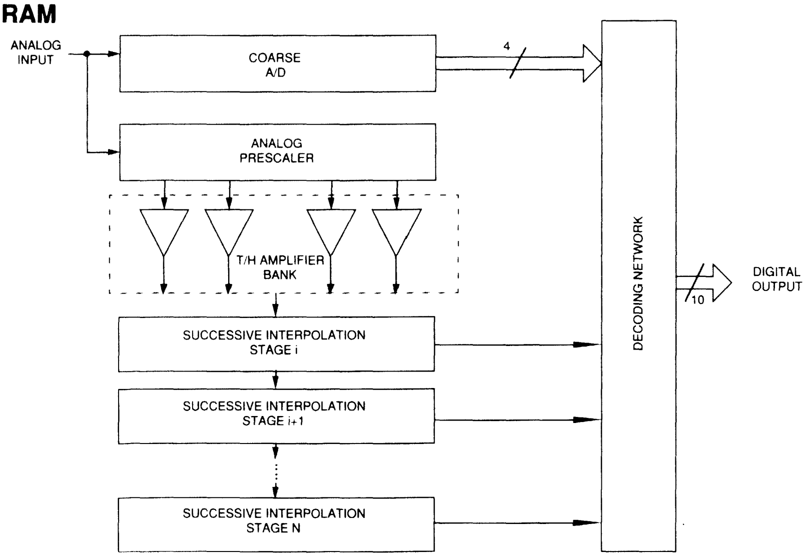
GENERAL DESCRIPTION

The SPT7820 A/D converter is a 10-bit monolithic converter capable of word rates of up to 30 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are TTL compatible to interface with both TTL and CMOS logic systems. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.0 watt with power supply voltages of +5.0 and -5.2 volts. The SPT7820 also provides a wide input voltage swing of ±2.0 volts.

The SPT7820 is available in a small 28-lead ceramic sidebrazed DIP package, LCC, and die form. An industrial temperature range of -25 to +85 °C is currently offered with military temperature and /883 processed units to be available in the near future.

BLOCK DIAGRAM

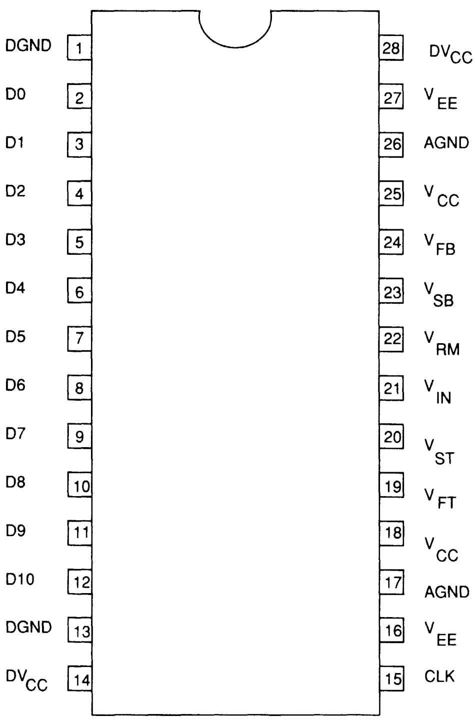


ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{ST}=+2.0 V, V_{SB}=-2.0 V, f_{clock}=20 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7820 MIN	TYP	MAX	UNITS
Analog Input						
Input Voltage Range		II		±2.0		V
Input Capacitance		V		5		pF
Maximum Conversion Rate		II	20			MHz
Dynamic Performance						
Signal-To-Noise Ratio (without Harmonics)						
fin=1 MHz		II		59		dB
fin=3.58 MHz		II		58		dB
fin=10.3 MHz		II		53		dB
Harmonic Distortion						
fin=1 MHz	64 Distortion BINS from 4096 pt FFT	II		59		dB
fin=3.58 MHz		II		58		dB
fin=10.3 MHz		II		48		dB
Total Dynamic Error						
fin=1 MHz		II		56		dB
fin=3.58 MHz		II		55		dB
fin=10.3 MHz		II		47		dB
Power Dissipation	Outputs Open	II		1.0	1.3	W

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	TTL Outputs (D0=LSB)
D10	TTL Output Overrange
CLK	Clock
V_{EE}	-5.2 V Supply
AGND	Analog Ground
V_{CC}	+5.0 V supply
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply (TTL Outputs)
V_{RM}	Middle of Voltage Reference Ladder
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

SIGNAL PROCESSING TECHNOLOGIES

SPT7824

10-BIT, 40 MSPS, TTL, A/D CONVERTER

ADVANCE INFORMATION

FEATURES

- Monolithic 40 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 57 dB SNR @ 3.58 MHz Input
- 50 dB SNR @ 10.3 MHz Input
- Low Power (1.0 W Typical)
- 5 pF input Capacitance
- TTL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

3

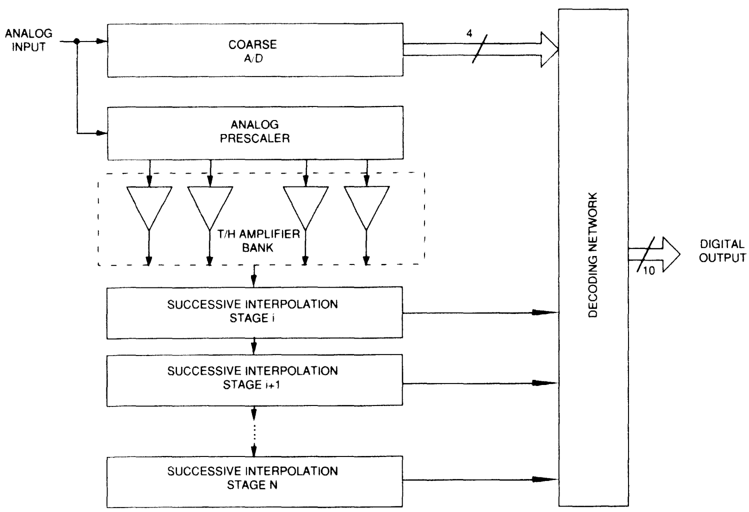
GENERAL DESCRIPTION

The SPT7824 A/D converter is a 10-bit monolithic converter capable of word rates of up to 50 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are TTL compatible to interface with both TTL and CMOS logic systems. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.0 watt with power supply voltages of +5.0 and -5.2 volts. The SPT7824 also provides a wide input voltage swing of ±2.0 volts.

The SPT7824 is available in a small 28-lead ceramic sidebrazed DIP package, LCC, and die form. An industrial temperature range of -25 to +85 °C is currently offered with military temperature and /883 processed units to be available in the near future.

BLOCK DIAGRAM

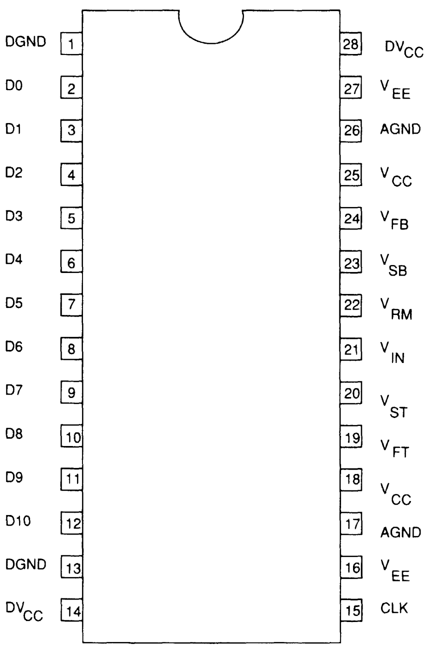


ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{ST}=+2.0 V, V_{SB}=-2.0 V, f_{clock}=40 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7824 MIN	TYP	MAX	UNITS
Analog Input						
Input Voltage Range		II		±2.0		V
Input Capacitance		V		5		pF
Maximum Conversion Rate		II	40			MHz
Dynamic Performance						
Signal-To-Noise Ratio (without Harmonics)						
fin=1 MHz		II		57		dB
fin=3.58 MHz		II		57		dB
fin=10.3 MHz		II		50		dB
Harmonic Distortion						
fin=1 MHz	64 Distortion BINS from 4096 pt FFT	II		56		dB
fin=3.58 MHz		II		56		dB
fin=10.3 MHz		II		48		dB
Total Dynamic Error						
fin=1 MHz		II		54		dB
fin=3.58 MHz		II		54		dB
fin=10.3 MHz		II		46		dB
Power Dissipation	Outputs Open	II		1.0	1.3	W

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	TTL Outputs (D0=LSB)
D10	TTL Output Overrange
CLK	Clock
V_{EE}	-5.2 V Supply
AGND	Analog Ground
V_{CC}	+5.0 V supply
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply (TTL Outputs)
V_{RM}	Middle of Voltage Reference Ladder
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

SIGNAL PROCESSING TECHNOLOGIES

SPT7910

12-BIT, 10 MHz, ECL, A/D CONVERTER

ADVANCE INFORMATION

FEATURES

- Monolithic
- 12-Bit 10 MSPS Converter
- 66 dB SNR @ 3.58 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.4 W Typical)
- 5 pF input Capacitance
- ECL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-optics

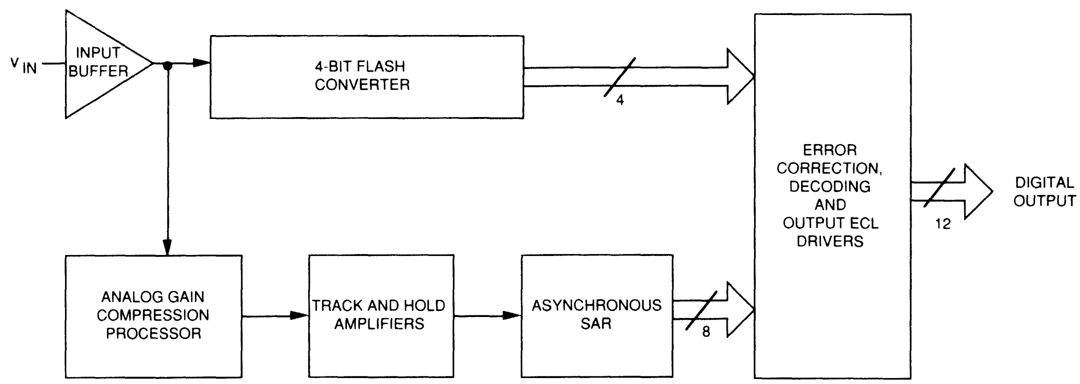
GENERAL DESCRIPTION

The SPT7910 A/D converter is industry's first 12-bit monolithic A-to-D converter capable of word rates greater than 10 MHz. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.4 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7910 also provides a wide input voltage range of ±2.0 volts.

The SPT7910 is available in a small 32-lead ceramic sidebrazed DIP package and in die form. An industrial temperature range of -25 to +85 °C is currently offered. LCC package, military temperature, and /883 processed units will be available in the near future.

BLOCK DIAGRAM

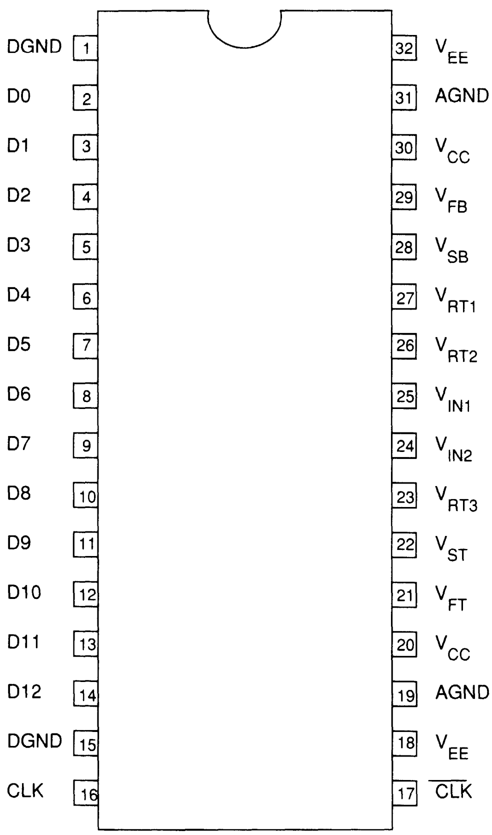


ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{ST}=+2.0 V, V_{SB}=-2.0 V, f_{clock}=10 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7910 MIN	TYP	MAX	UNITS
Analog Input						
Input Voltage Range		II		±2.0		V
Input Capacitance		V		5		pF
Maximum Conversion Rate		II	10			MHz
Dynamic Performance						
Signal-To-Noise Ratio (without Harmonics)						
	fin=1 MHz	II		68		dB
	fin=3.58 MHz	II		66		dB
Power Dissipation	Outputs Open	II		1.4	1.8	W

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	ECL Outputs (D0=LSB)
D12	ECL Output Overrange
CLK	Clock
$\overline{CLK}$	Inverted Clock
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1},V_{RT2},V_{RT3}	Voltage Reference Taps
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

SIGNAL PROCESSING TECHNOLOGIES

SPT7912

12-BIT, 20 MHz, ECL, A/D CONVERTER

ADVANCE INFORMATION

FEATURES

- Monolithic
- 12-Bit 20 MSPS Converter
- 66 dB SNR @ 3.58 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.4 W Typical)
- 5 pF input Capacitance
- ECL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-optics

3

GENERAL DESCRIPTION

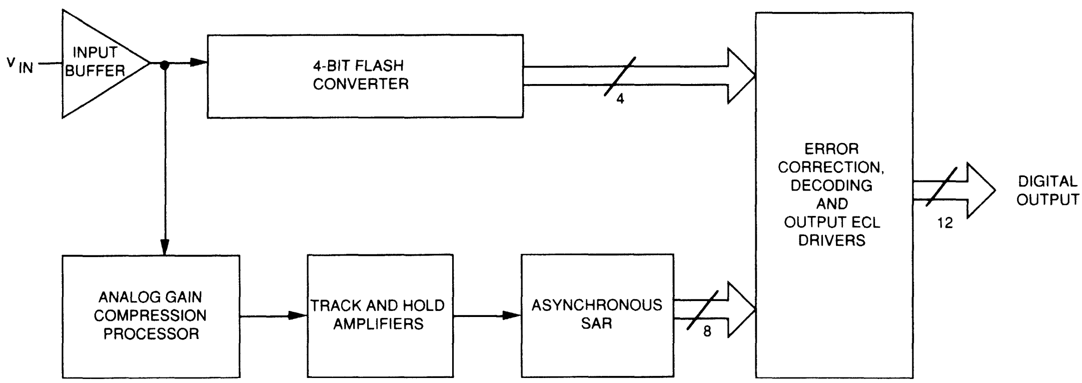
The SPT7912 A/D converter is industry's first 12-bit monolithic A-to-D converter capable of word rates greater than 20 MHz. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions.

Output data format is straight binary. Power dissipation is very low at only 1.4 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7912 also provides a wide input voltage range of ±2.0 volts.

The SPT7912 is available in a small 32-lead ceramic sidebrazed DIP package and in die form. An industrial temperature range of -25 to +85 °C is currently offered. LCC package, military temperature, and /883 processed units will be available in the near future.

BLOCK DIAGRAM

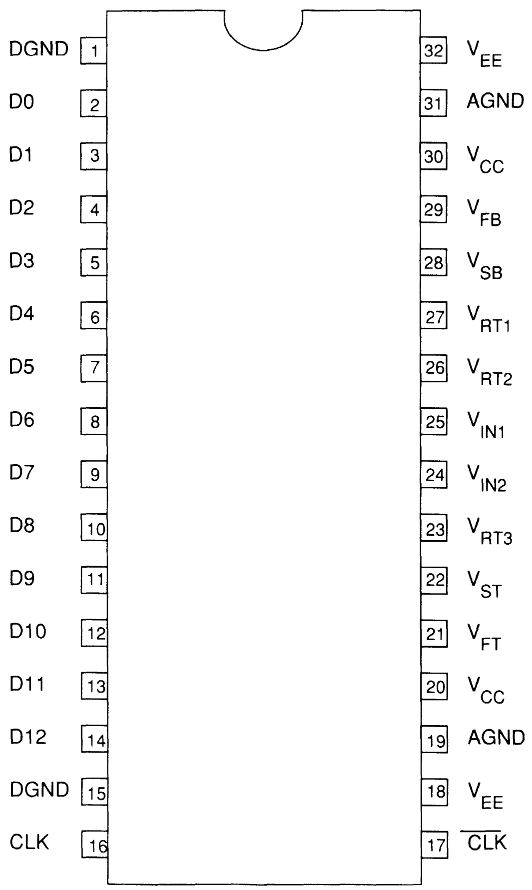


ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{ST}=+2.0 V, V_{SB}=-2.0 V, f_{clock}=20 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7912 MIN	SPT7912 TYP	SPT7912 MAX	UNITS
Analog Input						
Input Voltage Range		II		±2.0		V
Input Capacitance		V		5		pF
Maximum Conversion Rate		II	20			MHz
Dynamic Performance						
Signal-To-Noise Ratio (without Harmonics)						
	fin=1 MHz	II		68		dB
	fin=3.58 MHz	II		66		dB
	fin=10.3 MHz	II		56		dB
Power Dissipation	Outputs Open	II		1.4	1.8	W

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	ECL Outputs (D0=LSB)
D12	ECL Output Overrange
CLK	Clock
$\overline{CLK}$	Inverted Clock
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1},V_{RT2},V_{RT3}	Voltage Reference Taps
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

SIGNAL PROCESSING TECHNOLOGIES

SPT7920

12-BIT, 10 MHz, TTL, A/D CONVERTER

ADVANCE INFORMATION

FEATURES

- Monolithic
- 12-Bit, 10 MSPS Converter
- 66 dB SNR @ 3.58 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.1 W Typical)
- 5 pF input Capacitance
- TTL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-optics

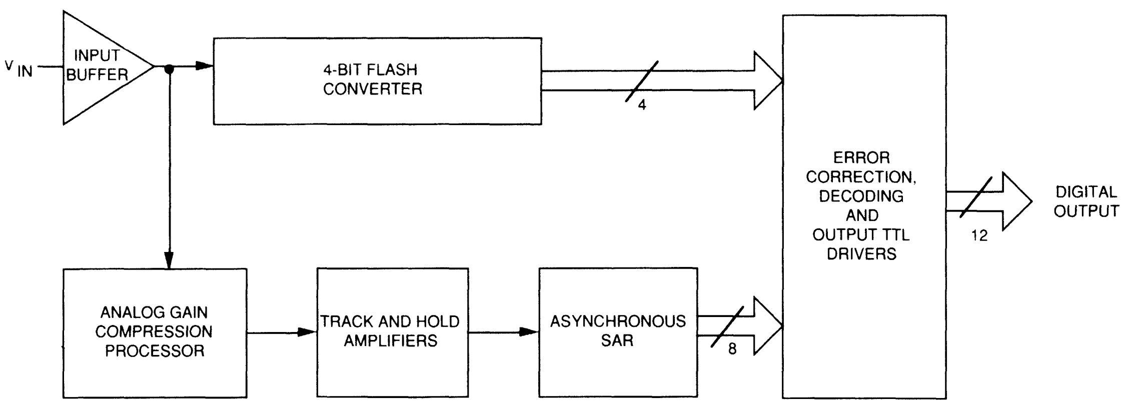
GENERAL DESCRIPTION

The SPT7920 A/D converter is industry's first 12-bit monolithic A-to-D converter capable of word rates greater than 10 MHz. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are TTL compatible to interface with both TTL and CMOS logic systems. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.1 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7920 also provides a wide input voltage range of ±2.0 volts.

The SPT7920 is available in a small 32-lead ceramic sidebrazed DIP package and in die form. An industrial temperature range of -25 to +85 °C is currently offered. LCC package, military temperature, and /883 processed units will be available in the near future.

BLOCK DIAGRAM

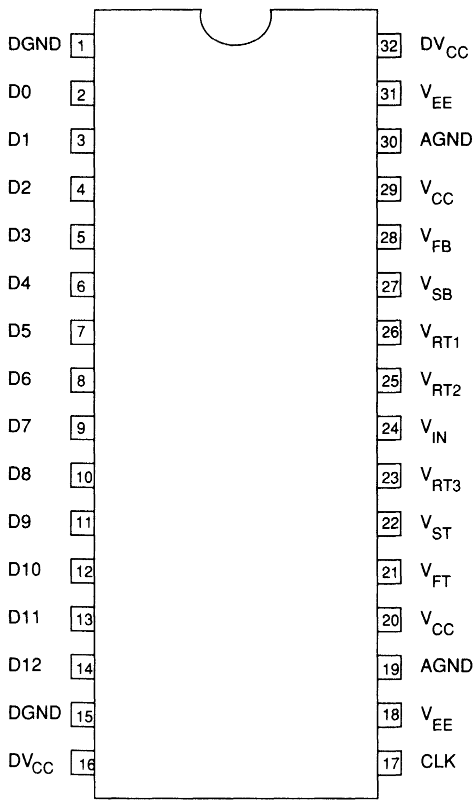


ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, DV_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{ST}=+2.0 V, V_{SB}=-2.0 V, f_{clock}=10 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7920 MIN	TYP	MAX	UNITS
Analog Input						
Input Voltage Range		II		±2.0		V
Input Capacitance		V		5		pF
Maximum Conversion Rate		II	10			MHz
Dynamic Performance						
Signal-To-Noise Ratio (without Harmonics)						
	fin=1 MHz	II		68		dB
	fin=3.58 MHz	II		66		dB
Power Dissipation	Outputs Open	II		1.1	1.5	W

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	TTL Outputs (D0=LSB)
D12	TTL Output Overrange
CLK	Clock
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1}-V_{RT3}	Voltage Reference Taps
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply (TTL Outputs)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

SIGNAL PROCESSING TECHNOLOGIES

SPT7922

12-BIT, 20 MHz, TTL, A/D CONVERTER

ADVANCE INFORMATION

3

FEATURES

- Monolithic
- 12-Bit, 20 MSPS Converter
- 66 dB SNR @ 3.58 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.1 W Typical)
- 5 pF input Capacitance
- TTL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-optics

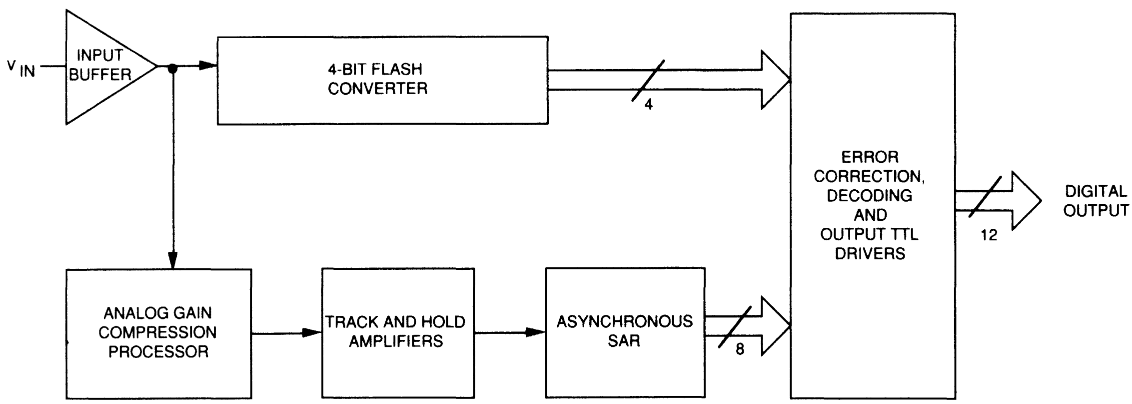
GENERAL DESCRIPTION

The SPT7922 A/D converter is industry's first 12-bit monolithic A-to-D converter capable of word rates greater than 20 MHz. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are TTL compatible to interface with both TTL and CMOS logic systems. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.1 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7922 also provides a wide input voltage range of ±2.0 volts.

The SPT7922 is available in a small 32-lead ceramic sidebrazed DIP package and in die form. An industrial temperature range of -25 to +85 °C is currently offered. LCC package, military temperature, and /883 processed units will be available in the near future.

BLOCK DIAGRAM

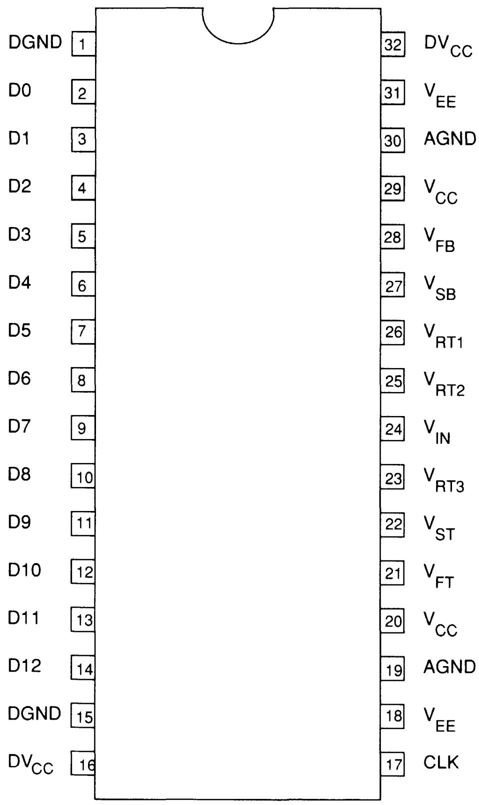


ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{CC}=+5.0 V, DV_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{ST}=+2.0 V, V_{SB}=-2.0 V, f_{clock}=20 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7922 MIN	TYP	MAX	UNITS
Analog Input						
Input Voltage Range		II		±2.0		V
Input Capacitance		V		5		pF
Maximum Conversion Rate		II	20			MHz
Dynamic Performance						
Signal-To-Noise Ratio (without Harmonics)						
	fin=1 MHz	II		68		dB
	fin=3.58 MHz	II		66		dB
	fin=10.3 MHz	II		56		dB
Power Dissipation	Outputs Open	II		1.1	1.5	W

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	TTL Outputs (D0=LSB)
D12	TTL Output Overrange
CLK	Clock
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1}-V_{RT3}	Voltage Reference Taps
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply (TTL Outputs)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

HDAC7542A

CMOS, 12-BIT MICROPROCESSOR BUFFERED DAC

SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- Improved Version of the AD7542
- Maximum Gain Error <1/2 LSB (A/G Grade)
- 500 ns Settling Time
- 12-Bit Linearity Over Temperature
- Microprocessor Compatible I/O
- Low Gain Drift (<3 ppm/°C)
- 4-Quadrant Multiplication

APPLICATIONS

- μP Controlled Gain Circuits
- μP Controlled Function Generation
- Bus Structured Instruments
- μP Based Control Systems
- μP Attenuator Control

4

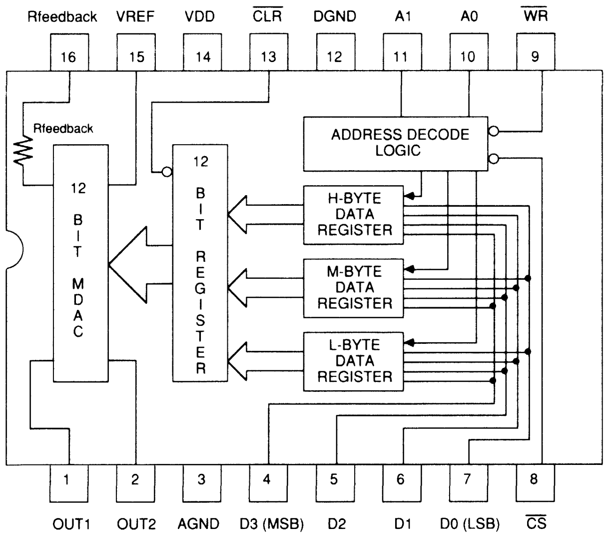
GENERAL DESCRIPTION

The HDAC7542A is a monolithic, low cost, multiplying 12-bit digital-to-analog converter (DAC) designed for direct microprocessor interface. It is compatible with the industry standard 7542 but has significant performance improvements in speed and gain accuracy. The HDAC7542A is fabricated in a three-micron, polysilicon gate BEMOS process and operates from a single +5 V (maximum) supply. Excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is ensured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes for latch-up protection.

The data bits for selecting the DAC output are written into the HDAC7542A via a direct connection to the parallel bus of a microprocessor. Data bytes are written as 3, 4-bit groups or nibbles into the data registers on the chip. This input bits are double buffered on chip. Updating the analog output is controlled via the paralled bus by writing to the chip. A clear pin ($\overline{CLR}$) allows for resettling the output to all zeros under power-up or system reset conditions. All address decoding for writing to the chip registers is handled on the chip.

The HDAC7542's direct parallel bus interconnect makes it an excellent choice for microprocessor-based instruments and industrial or process controllers utilizing microprocessors.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{DD} to GND .... +7 V

AGND to GND .... -0.3 to V_{DD}

Input Voltages

$V_{Rfeedback}$ to GND .... ±25 V

Digital Input Voltage to GND .... 0.3 to V_{DD}

Outputs

V_{OUT1} or V_{OUT2} to GND .... -0.3 V to V_{DD}

Temperature

Operating Temperature, ambient............... -55 to +125 °C

junction......................... +150 °C

Lead Temperature, (soldering 10 seconds)........ +300 °C

Storage Temperature............................... -65 to +150 °C

Power Dissipation (Any Package) to +75 °C........ 450mW

(Derates above +75 °C by 6 mW/°C)

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal appliied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=OUT2=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G MIN	NOM	MAX	HDAC7542AA MIN	NOM	MAX	HDAC7542AB MIN	NOM	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		I		12			12			12		Bits
Relative Accuracy		I	-.5	±.25	+.5	-.5		+.5	-1		+1	LSB
Differential Nonlinearity		I	-.5	±.25	+.5	-.5		+.5	-1		+1	LSB
Gain Error	25 °C	I	-.5		+.5	-2		+2	-3		+3	LSB
Using Internal $R_{feedback}$	Tmin - Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Gain Temperature Coefficient		IV		0.3	3		0.3	3		0.3	3	ppm/°C
Output Leakage OUT1[4]												
and OUT2	25 °C	I	-1		+1	-1		+1	-1		+1	nA
	0-70 °C/-25 to +85 °C	I	-10		+10	-10		+10	-10		+10	nA
	-55 to +125 °C	I	-50		+50	-50		+50	-50		+50	nA
	All digital inputs at 0 V											
Reference Input Resistance	Pin 19 to GND											
	+25 °C	IV	7	12.5	18	7	12.5	18	7	12.5	18	kΩ
	Temp. Coefficient	IV		-180			-180			-180		ppm/°C
DIGITAL INPUTS												
V_{IH} (High Input Voltage)		I	2.4			2.4			2.4			V
V_{IL} (Low Input Voltage)		I			0.8			0.8			0.8	V
I_{IN} (Input Currents I_{IH}, I_{IL})		I			±1			±1			±1	µA
C_{IN} (Input Capacitance)	VIN=0 Volts	IV			5			5			5	pF

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G MIN	HDAC7542AA/G NOM	HDAC7542AA/G MAX	HDAC7542AA MIN	HDAC7542AA NOM	HDAC7542AA MAX	HDAC7542AB MIN	HDAC7542AB NOM	HDAC7542AB MAX	UNITS
I_{DD}	Logic Inputs at V_{IL} or V_{IH}	I			2.5			2.5			2.5	mA
AC ELECTRICAL CHARACTERISTICS												
Multiplying Feedthrough Error	V_{REF} to V_{OUT} V_{REF}=±10 V 10 kHz Sinewave	IV		0.3	0.5		0.3	0.5		0.3	0.5	mV(p-p)
Output Current Settling Time[1,3]		IV		0.5	1.0		0.5	1.0		0.5	1.0	µsec
Capacitance OUT1,2	Digital Inputs=V_{IH}	IV			75			75			75	pF
Capacitance OUT1,2	Digital Inputs=V_{IL}	IV			30			30			30	pF
SWITCHING CHARACTRISTICS												
t_{WR} (WRITE Pulse Width)		I	40			40			40			nsec
t_{AWH} (Address-to-WRITE hold time)		I	0			0			0			nsec
t_{CWH} (Chip select-to-WRITE hold Time)		I	0			0			0			nsec
t_{CLR} (Clear pulse Width)		I	40			40			40			nsec
INPUT BYTE REGISTER LOADING												
t_{CWS} (Chip select-to-WRITE Setup Time)		I	0			0			0			nsec
t_{AWS} (Address Valid-to-WRITE Setup Time)		I	40			40			40			nsec
t_{DS} (Data Setup Time)		I	20			20			20			nsec
t_{DH} (Data Hold Time)		I	20			20			20			nsec
INTERNAL DAC REGISTER LOADING												
t_{CWS} (Chip Select-to-WRITE Setup Time)		I	0			0			0			nsec
t_{AWS} (Address Valid-to-WRITE Setup Time)		I	40			40			40			nsec

Note 1: OUT1 load: 100 Ω + 13 pF
Note 2: Digital inputs change from 0 V to V_{DD} or V_{DD} to 0 V
Note 3: Measured from falling edge of $\overline{WR}$.
Note 4: Digital inputs $\overline{WR}$ and $\overline{CS}$ at 0 V.

TEST LEVEL CODES

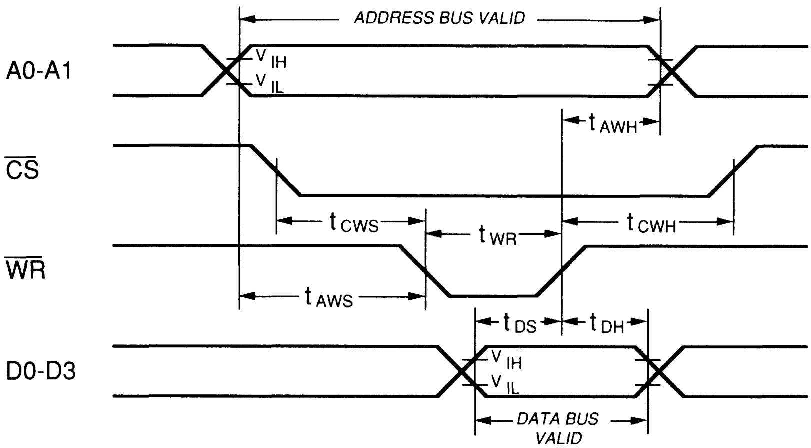
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Figure 1 - Write Cycle Timing Diagram



TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in percentage of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7542A ideal full-scale output is -(4095)/(4096)•(V_{REF}). Gain error is adjustable to zero using external trims as shown in figures 6 and 7, and Table 1.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0s, or OUT2 with the DAC loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the V_{REF} terminal to OUT1 with the DAC loaded to all 0s.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

CIRCUIT DESCRIPTION

As shown in the block diagram, the HDAC7542A consists of a 12 bit multiplying DAC and data input logic. The data input logic consists of three 4-bit input data registers (H, M and L-Byte) and a 12-bit DAC register. The DAC register is loaded from the three input registers. Content of the DAC register controls the DAC's analog output level. Data entry is further described in the Interface Logic section.

Figure 2A shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7542A uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7542A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the remaining VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switches route the bit-weighted current of the leg to either analog ground (pin OUT2) or to the output (pin OUT1). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the three most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7542A is identical to similar devices that use an unmodified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the external resistor shown in Figure 2A in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered VOUT, and in combination with the feedback resistance maintains OUT1 at virtual ground. The transfer function of Figure 2B shows the relationship of VOUT for an equivalent R-2R resistor network, shown in the same figure. A more detailed explanation of the circuit operation and performance aspects is found in the following Equivalent Circuit Analysis section.

Figure 2A - Simplified Circuit Desription

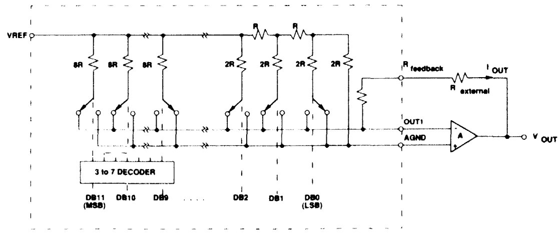
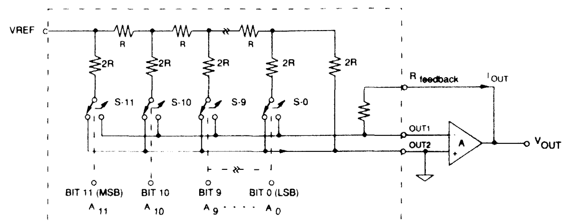


Figure 2B - Equivalent R-2R Resistor Network



The transfer function for the HDAC7542A connected in the multiplying mode as shown in Figure 2B is:

$$V_{OUT} = V_{REF} \times \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \cdots + \frac{A_0}{2^{12}} \right)$$

in which A_x assumes a value of 1 for a HIGH bit and 0 for a Low bit.

EQUIVALENT CIRCUIT ANALYSIS

The equivalent output circuit of the HDAC7542A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects. In Figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to OUT2. OUT2 is internally connected to AGND in packaged versions of the HDAC7542A. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin V_{REF} plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in figures 3 and 4.

Figure 3 - HDAC7542A DAC Equivalent Circuit All Digital Inputs Low

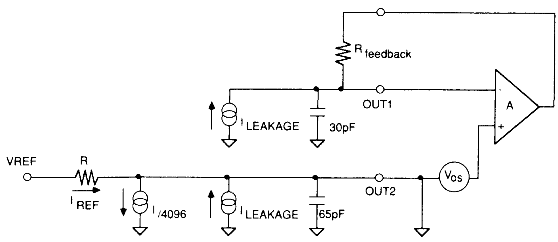
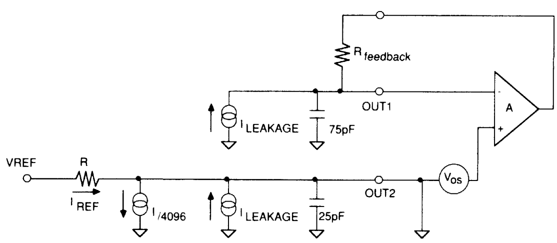


Figure 4 - HDAC7542A DAC Equivalent Circuit All Digital Inputs High



The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between figures 3 and 4, resistance at each op-amp input can change from 10k Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below:

Offset gain=1 + $R_{feedback}$/RDAC

With all code bits LOW:
RDAC >> $R_{feedback}$; offset gain=1

With all code bits HIGH:
RDAC= $R_{feedback}$; offset gain=2

Thus, the offset is not amplified by a constant gain over the range of code input. This variation in offset gain is seen as a nonlinearity in the voltage output over the full scale output. The magnitude of nonlinearity is the difference in the gains at code extremes times the offset voltage. In this DAC, this nonlinearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (figures 6 and 7). Although all R-2R DAC's have the need for this type of compensation, the HDAC7542A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7542A.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.

- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp: as a rule of thumb, about one half of the op-amp's gain-bandwidth.

- Settling time is proportional to $\sqrt{C_{OUT\,1} + C1}$.

For an OP-17 used as an output op-amp with 8 MHz gain-bandwidth, the choice of C1 is:

$(2 \cdot \pi \cdot C1 \cdot R_{feedback})^{-1}$= 15 MHz or C1= 15 pf

$\cdot R_{feedback}$ = 12.5 kΩ

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7542A 's low output capacitance comes much closer to fulfilling this goal than most other 7542 compatible DAC's. Thus, faster, more well controlled settling is seen with the HDAC7542A.

Table I - Input Logic Truth Table

HDAC7542A CONTROL INPUTS					HDAC7542A OPERATION
A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$	
X	X	X	X	0	RESETS DAC REGISTER TO 0000 0000 0000 (1)
X	X	1	X	1	NO OPERATION, DEVICE NOT SELECTED
0	0	0	↑ (positive edge)	1	LOAD L-BYTE DATA REGISTER WITH DATA AT D0-D3
0	1	0	↑ (positive edge)	1	LOAD M-BYTE DATA REGISTER WITH DATA AT D0-D3
1	0	0	↑ (positive edge)	1	LOAD H-BYTE DATA REGISTER WITH DATA AT D0-D3
1	1	0	⊔ (level)	1	LOAD DAC REGISTER WITH L, M, H-BYTE REG. DATA

NOTE (1) :
CLR = 0 ASYNCHRONOUSLY RESETS
DAC REGISTER TO 0000 0000 0000 BUT
HAS NO EFFECT ON INPUT REGISTERS.

0 = LOGIC LOW
1 = LOGIC HIGH
X = DON'T CARE
↑ = POSITIVE EDGE TRIGGERED
⊔ = LEVEL TRIGGERED

INTERFACE LOGIC

Data is loaded into the HDAC7542A in three 4-bit bytes through data pins D0, D1, D2, and D3. Address pins A0 and A1 select the loading of internal byte register H (high byte), M (middle Byte) or L (low byte). Address pins A0 and A1 also allow the selection of the internal 12-bit DAC register, which is loaded by the H, M and L register simultaneously. Data in the internal DAC register determines the DAC analog output value. Table 1 above provides the complete input logic truth table.

Write timing, as shown in the Write Cycle Timing Diagram, is similar to data loading of a RAM device. Note that pin $\overline{WR}$ is used to both load the input byte registers and the internal DAC register. The $\overline{CLR}$ pin, when momentarily brought to logic 0, resets the internal DAC register to 0000 0000 0000. This feature is useful for system initialization since the DAC output is set to a known condition.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

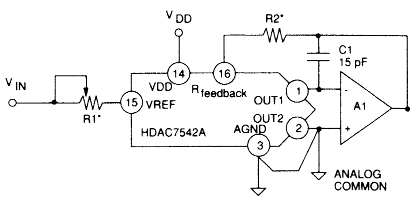
Figure 6 illustrates the use of the HDAC7542A in a unipolar (or 2 quadrant multiplication) mode. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the V_{REF} voltage out. If the source of V_{REF} is adjustable, V_{REF} could be directly adjusted for full scale calibration. (See Table III.)

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

The op-amp used with the HDAC7542 should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the offset effect which is code dependent and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

Figure 6 - Unipolar Binary Operation



* REFER TO TABLE III

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7542A in a bipolar (or 4 quadrant multiplication) mode is illustrated in figure 7. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of V_{REF} to produce a maximum output which is half of V_{REF} in either polarity (see Table IV for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the V_{REF} source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track each other for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate the OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

Table II - Recommended Trim Resistor Values vs Grades

TRIM RESISTOR	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

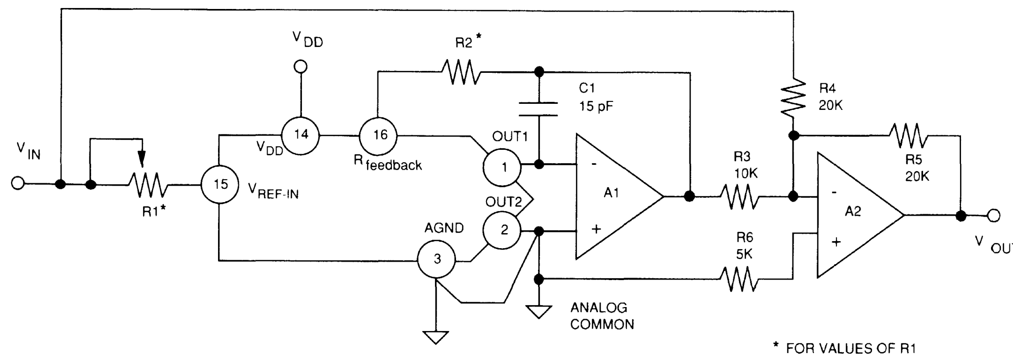
Table III - Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

Table IV- Bipolar Binary Code Table for Circuit of Figure 5

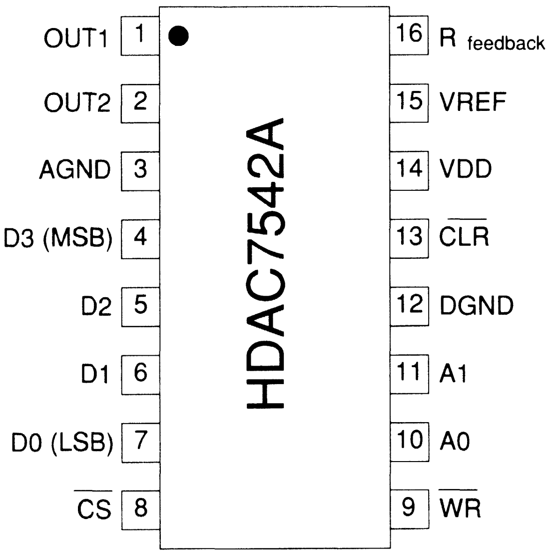
BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Figure 7 - Bipolar Operation



* FOR VALUES OF R1 AND R2 SEE TABLE I.

PIN ASSIGNMENT HDAC7542A



PIN FUNCTIONS HDAC7542A

NAME	FUNCTION
OUT1	Analog Current Output 1
OUT2	Analog Current Output 2
AGND	Analog Ground
D3	Data Bus Input 3 (MSB)
D2	Data Bus Input 2
D1	Data Bus Input 1
D0	Data Bus Input 0 (LSB)
$\overline{CS}$	Chip Select Input
$\overline{WR}$	Data Write Input
A0	Address Bus Input 0
A1	Address Bus Input 1
DGND	Digital Ground
$\overline{CLR}$	Clear Input for DAC Reg
VDD	Positive Power Supply
VREF	Reference Input Voltage
$R_{feedback}$	Internal Feedback Resistor

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

HDAC7543A

CMOS, 12-BIT SERIAL INPUT BUFFERED MULTIPLYING DAC

SPT SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- Improved Version of the AD7543
- Max Gain Error <1/2 LSB (A/G Grade)
- 500 ns Settling Time
- 12-Bit Linearity Over Temperature
- Low Gain Drift (<3 ppm/°C)
- Serial Data Load With Flexible Strobe Conditions
- Four Quadrant Multiplication

APPLICATIONS

- Proportional Controllers Requiring Serial Isolation or Remote Location
- Industrial and Process Controllers

GENERAL DESCRIPTION

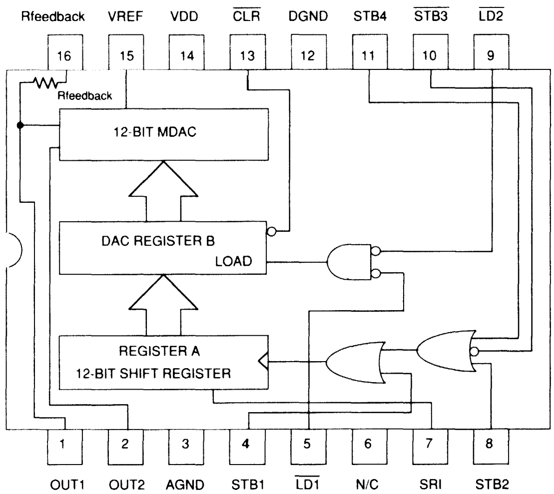
The HDAC754A is a monolithic, low cost, multiplying 12-bit digital-to-analog converter (DAC) designed for serial digital input. It is compatible with the industry standard 7542 but has significant performance improvements in speed and gain accuracy. The HDAC7543A is fabricated in a three-micron, polysilicon gate BEMOS process and operates from a single +5 V (maximum) supply. Excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is ensured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes for latch-up protection.

The data bits for selecting the DAC output are written into the HDAC7543A via a serial data port prior to latching them into the output register. The input bits are double buffered on-chip. The serial bus control pins provide a great deal of flexibility in providing the serial input strobe conditions for the data transfer. A clear pin ($\overline{CLR}$) allows for resettling the output to all zeros under power up or system reset conditions.

The HDAC7543A's direct serial data interconnect makes it an excellent choice for industrial or process controllers which require electrical isolation or remote location. The serial bus minimizes the number of control lines which would require isolation devices or line drivers in these types of applications.

4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
V_{DD} to GND ....+7 V
AGND to GND ....-0.3 to V_{DD}
Input Voltages
$V_{Rfeedback}$ to GND ....±25 V
Digital Input Voltage to GND ....0.3 to V_{DD}
Outputs
V_{out1} or V_{out2} to GND ....-0.3 V to V_{DD}

Temperature
Operating Temperature, ambient............... -55 to +125 °C
junction......................... +150 °C
Lead Temperature, (soldering 10 seconds)........ +300 °C
Storage Temperature................................ -65 to +150 °C
Power Dissipation (Any Package) to +75 °C........ 450mW
(Derates above +75 °C by 6 mW/°C)

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal appliied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=OUT2=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G MIN	HDAC7543AA/G NOM	HDAC7543AA/G MAX	HDAC7543AA MIN	HDAC7543AA NOM	HDAC7543AA MAX	HDAC7543AB MIN	HDAC7543AB NOM	HDAC7543AB MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		I		12			12			12		Bits
Relative Accuracy		I	-.5	±.25	+.5	-.5		+.5	-1		+1	LSB
Differential Nonlinearity		I	-.5	±.25	+.5	-.5		+.5	-1		+1	LSB
Gain Error	25 °C	I	-.5		+.5	-2		+2	-3		+3	LSB
Using Internal $R_{feedback}$	Tmin - Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Gain Temperature Coefficient		IV		0.3	3		0.3	3		0.3	3	ppm/°C
Output Leakage OUT1[4]												
A and OUT2	25 °C	I	-1		+1	-1		+1	-1		+1	nA
	0-70 °C/-25 to +85 °C	I	-10		+10	-10		+10	-10		+10	nA
	-55 to +125 °C	I	-50		+50	-50		+50	-50		+50	nA
	All digital inputs at 0 V											
Reference Input Resistance	Pin 15 to GND											
	+25 °C	IV	7	12.5	18	7	12.5	18	7	12.5	18	kΩ
	Temp. Coefficient	IV		-180			-180			-180		ppm/°C
DIGITAL INPUTS												
V_{IH} (High Input Voltage)		I	2			2			2			V
V_{IL} (Low Input Voltage)		I			0.8			0.8			0.8	V
I_{IN} (Input Currents I_{IH}, I_{IL})		I			±1			±1			±1	µA
C_{IN} (Input Capacitance)	VIN=0 Volts	IV			5			5			5	pF

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=OUT2=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS		TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G MIN	HDAC7543AA/G NOM	HDAC7543AA/G MAX	HDAC7543AA MIN	HDAC7543AA NOM	HDAC7543AA MAX	HDAC7543AB MIN	HDAC7543AB NOM	HDAC7543AB MAX	UNITS
AC ELECTRICAL CHARACTERISTICS													
Multiplying Feedthrough Error		V_{REF} to V_{OUT} V_{REF}=±10 V 10 kHz Sinewave	IV		0.3	0.5		0.3	0.5		0.3	0.5	mV(p-p)
Output Current Settling Time[1,3]			IV		0.5	1.0		0.5	1.0		0.5	1.0	µsec
Capacitance OUT1		Digital Inputs=V_{IH} $\overline{WR}$=$\overline{CS}$=0 V	IV			75			75			75	pF
Capacitance OUT2		Digital Inputs=V_{IL} $\overline{WR}$=$\overline{CS}$=0 V	IV			30			30			30	pF
Power Supply Rejection Ratio		+25 °C	I			.005			.005			.005	%
		Over Temperature	I			.01			.01			.01	%
Serial Input	t_{DS1}	STB1 Strobed	I	50			50			50			nsec
to Strobe	t_{DS2}	STB2 Strobed	I	20			20			20			nsec
Setup Time	t_{DS3}	$\overline{STB3}$ Strobed	I	0			0			0			nsec
	t_{DS4}	STB4 Strobed	I	0			0			0			nsec
Serial Input	t_{DH1}	STB1 Strobed	I	30			30			30			nsec
to Strobe	t_{DH2}	STB2 Strobed	I	60			60			60			nsec
Hold Time	t_{DH3}	$\overline{STB3}$ Strobed	I	80			80			80			nsec
	t_{DH4}	STB4 Strobed	I	80			80			80			nsec
t_{SRI} (SRI Data Pulse Width)			I	80			80			80			nsec
t_{STB1} (STB1 Pulse Width)			I	40			40			40			nsec
t_{STB2} (STB2 Pulse Width)			I	40			40			40			nsec
t_{STB3} ($\overline{STB3}$ Pulse Width)			I	40			40			40			nsec
t_{STB4} (STB4 Pulse Width)			I	40			40			40			nsec
$t_{LD1, LD2}$ (Load Pulse Width)			I	120			120			120			nsec
t_{ASB} (Min. Time Between Strobing LSB into Register A and Loading Register B			IV	0			0			0			nsec
t_{CLR} ($\overline{CLR}$ Pulse Width)			I	100			100			100			nsec

Note 1: OUT1 load: 100 Ω + 13 pF.
Note 2: Digital inputs change from 0 V to V_{DD} or V_{DD} to 0 V.
Note 3: Measured from falling edge of $\overline{WR}$.
Note 4: Digital inputs $\overline{WR}$ and $\overline{CS}$ at 0 V.
Note 5: Measured from falling edge of $\overline{WR}$ to 90% of final output value.

TEST LEVEL CODES

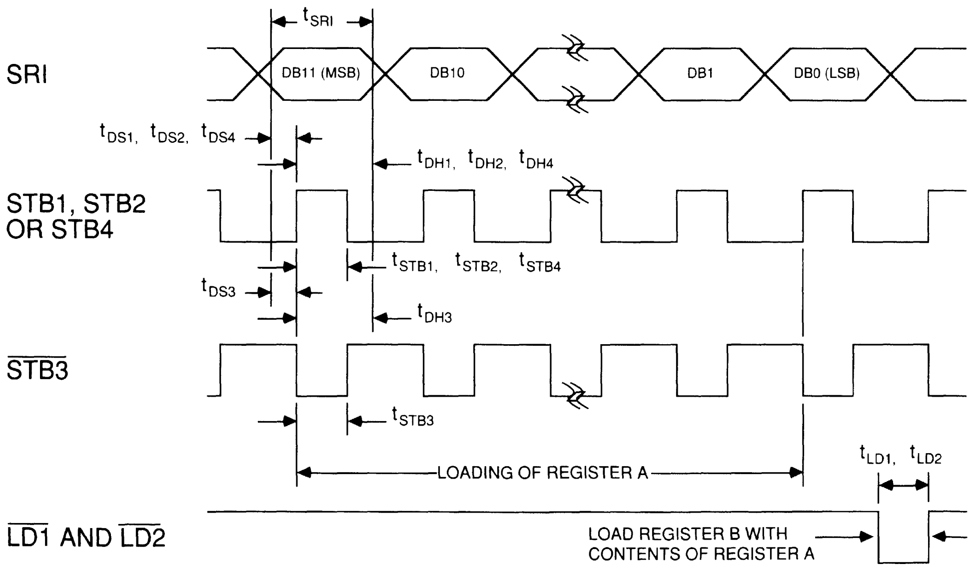
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Figure 1 - Logic Timing Diagram



TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in percentage of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7543A ideal full-scale output is $-(4095)/(4096) \cdot (V_{REF})$. Gain error is adjustable to zero using external trims as shown in figures 6 and 7.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0s, or OUT2 with the DAC loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the V_{REF} terminal to OUT1 with the DAC loaded to all 0s.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

CIRCUIT DESCRIPTION

As shown in the block diagram, the HDAC7543A consists of a 12 bit multiplying DAC and data input logic. The data input logic consists of a serial input data register (register A) and a parallel DAC register (register B). Register A loads register B with a 12-bit parallel data work. The content of register B controls the DAC's output. Data entry is further described in the Interface Logic section.

Figure 2A shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7543A uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7543A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the remaining VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switches route the bit-weighted current of the leg to either analog ground or to the output (pin OUT1). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the three most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7543A is identical to similar devices that use an unmodified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the external resistor shown in Figure 2A in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered VOUT, and in combination with the feedback resistance maintains OUT1 at virtual ground. The transfer function of Figure 2B shows the relationship of VOUT for an equivalent R-2R resistor network, shown in the same figure. A more detailed explanation of the circuit operation and performance aspects is found in the following Equivalent Circuit Analysis section.

Figure 2A - Simplified Circuit Description

Figure 2B - Equivalent R-2R Network

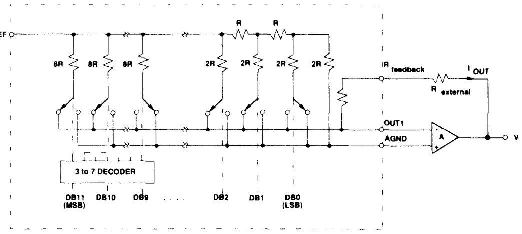
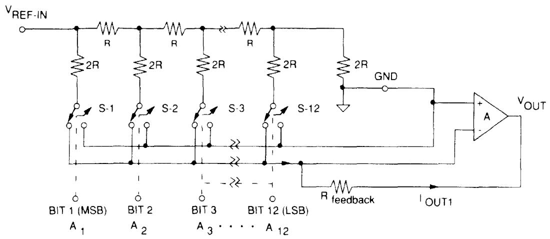


Figure 2B - Equivalent R-2R Network



The transfer function for the HDAC7543A connected in the multiplying mode as shown in figure 2B is:

$$V_O = -V_{REF} \times \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \frac{A_9}{2^3} \bullet \bullet \bullet \frac{A_0}{2^{12}} \right)$$

in which A_x assumes a value of 1 for a HIGH bit and 0 for a Low bit.

EQUIVALENT CIRCUIT ANALYSIS

The equivalent output circuit of the HDAC7543A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects.

In figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to OUT2. OUT2 is internally connected to AGND in packaged versions of the HDAC7543A. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin V_{REF} plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in figures 3 and 4.

Figure 3 - HDAC7543A DAC Equivalent Circuit All Digital Inputs Low

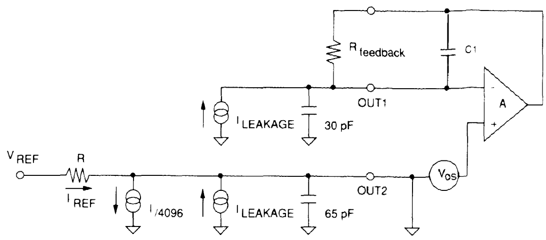
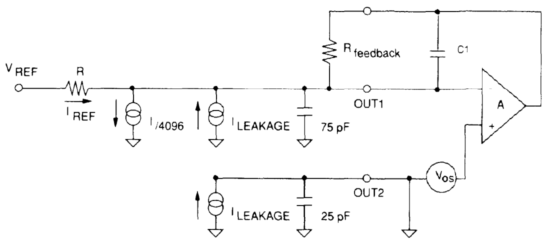


Figure 4 - HDAC7543A DAC Equivalent Circuit All Digital Inputs High



The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between figures 3 and 4, resistance at each op-amp input can change from 10k Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below:

Offset gain=1 + $R_{feedback}$/RDAC

With all code bits LOW:
RDAC >> $R_{feedback}$; offset gain=1

With all code bits HIGH:
RDAC= $R_{feedback}$; offset gain=2

Thus, the offset is not amplified by a constant gain over the range of code input. This variation in offset gain is seen as a nonlinearity in the voltage output over the full scale output. The magnitude of nonlinearity is the difference in the gains at code extremes times the offset voltage. In this DAC, this nonlinearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (figures 6 and 7). Although all R-2R DAC's have the need for this type of compensation, the HDAC7543A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7543A.

The choice of compensation capacitor is bounded by three limits:

• C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.

• The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp: as a rule of thumb, about one half of the op-amp's gain-bandwidth.

• Settling time is proportional to $\sqrt{C_{OUT\,1} + C1}$.

For an OP-27 used as an output op-amp with 8 MHz gain-bandwidth, the choice of C1 is:

$(2 \cdot \pi \cdot C1 \cdot R_{feedback})^{-1} = 15$ MHz or C1= 15 pf

$\cdot R_{feedback} = 12.5\ k\Omega$

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7543A 's low output capacitance comes much closer to fulfilling this goal than most other 7545 compatible DAC's. Thus, faster, more well controlled settling is seen with the HDAC7543A.

Table 1 - Input Logic Truth Table

REGISTER A CONTROL INPUTS				REGISTER B CONTROL INPUTS			HDAC7543A OPERATION
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$	
0	1	0	↑	X	X	X	DATA APPEARING AT SRI IS STROBED INTO REGISTER A (MSB FIRST)
0	1	↑	0	X	X	X	
0	↓	0	0	X	X	X	
↑	1	0	0	X	X	X	
1	X	X	X				NO OPERATION OF REGISTER A
X	0	X	X				
X	X	1	X				
X	X	X	1				
				0	X	X	SET REG. B TO 0000 0000 0000 (1)
				1	1	X	NO OPERATION OF REGISTER B
				1	X	1	
				1	0	0	LOAD REG. B WITH CONTENTS OF REG. A

NOTE (1):
CLR = 0 ASYNCHRONOUSLY RESETS
REGISTER B TO 0000 0000 0000
BUT HAS NO EFFECT ON REGISTER A.

0 = LOGIC LOW
1 = LOGIC HIGH
X = DON'T CARE
↑ = POSITIVE EDGE
↓ = NEGATIVE EDGE

INTERFACE LOGIC

Data is loaded into the HDAC7543A serially through pin SRI. The serial data is clocked into register A with either pin STB1, STB2 or STB4 at the rising clock edge or with pin $\overline{STB3}$ at the falling clock edge. When register A has been loaded with the 12 data bits, the data is transferred to register B by bringing both pin $\overline{LD1}$ and $\overline{LD2}$ momentarily low. Refer to the Logic Timing Diagram for loading sequence.

When pin $\overline{CLR}$ is momentarily brought to logic 0, register B is reset to 0000 0000 0000. This feature is useful for system initialization since the DAC output is set to a known condition.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

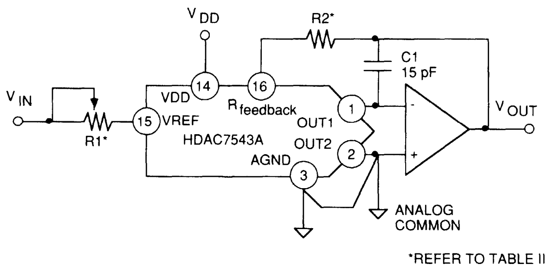
Figure 6 illustrates the use of the HDAC7543A in a unipolar (or 2 quadrant multiplication) mode. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the V_{REF} voltage out. If the source of V_{REF} is adjustable, V_{REF} could be directly adjusted for full scale calibration. (See Table II.)

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

The op-amp used with the HDAC5743A should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the offset effect which is code dependent and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

Figure 6 - Unipolar Binary Operation



BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7543A in a bipolar (or 4 quadrant multiplication) mode is illustrated in figure 7. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of V_{REF} to produce a maximum output which is half of V_{REF} in either polarity (see Table III for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the V_{REF} source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track each other for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate the OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

Table II - Recommended Trim Resistor Values vs Grades

TRIM RESISTOR	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

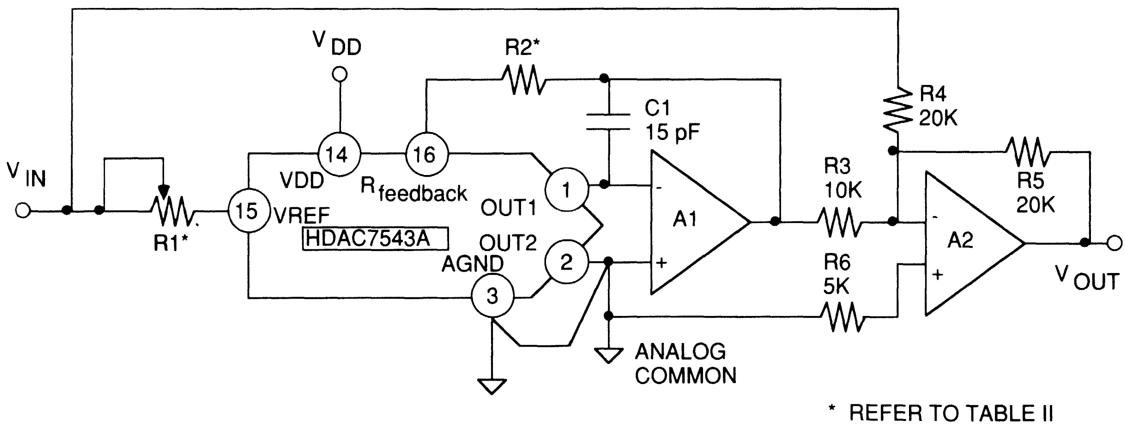
Table III - Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

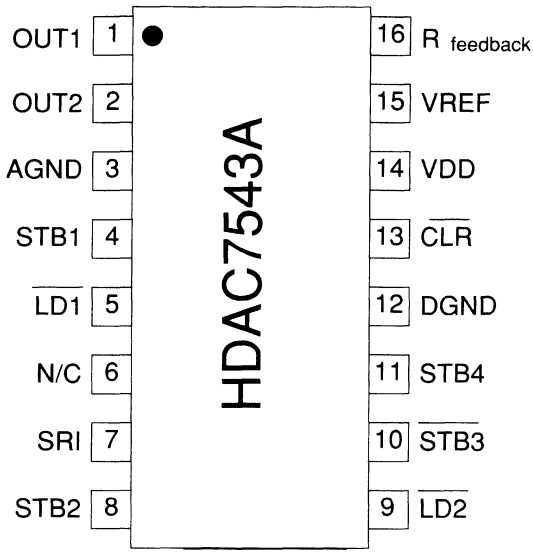
Table IV - Bipolar Binary Code Table for Circuit of Figure 5

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Figure 7 - Bipolar Operation



PIN ASSIGNMENT HDAC7543A



PIN FUNCTIONS HDAC7543A

NAME	FUNCTION
OUT1	Analog Current Output 1
OUT2	Analog Current Output 2
AGND	Analog Ground
STB1	Strobe Input 1 for Reg A
$\overline{LD1}$	Load Input 1 for Reg B
N/C	No Connection
SRI	Serial Data Input
STB2	Strobe Input 2 for Reg A
$\overline{LD2}$	Load Input 2 for Reg B
STB3	Strobe Input 3 for Reg A
STB4	Strobe Input 4 for Reg A
DGND	Digital Ground
$\overline{CLR}$	Clear Input for Reg B
VDD	Positive Power Supply
VREF	Reference Input Voltage
$R_{feedback}$	Internal Feedback Resistor

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SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

HDAC7545A

CMOS, 12-BIT BUFFERED MULTIPLYING DAC

SPT SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- Improved Version of the AD7545
- Low Gain Error <2 LSB
- Low Output Capacitance (<75 pF)
- 500 ns Settling Time
- 12-Bit Linearity Over Temperature
- 8 or 16-Bit Bus Compatibility

APPLICATIONS

- μP Controlled Gain Circuits
- μP Controlled Function Generation
- Bus Structured Instruments
- μP Based Control Systems

4

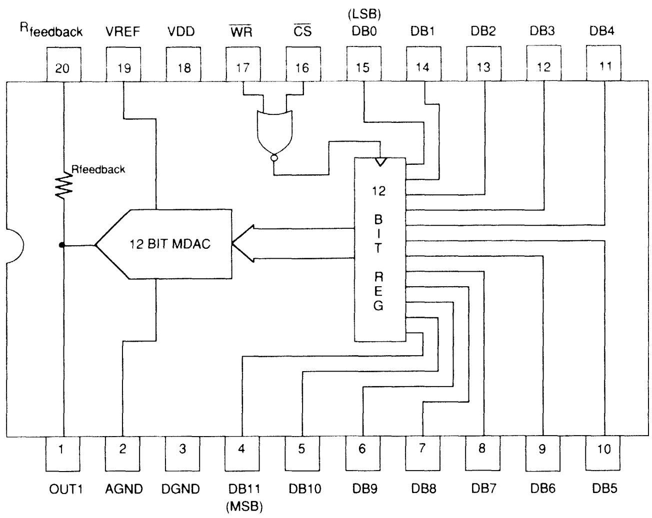
GENERAL DESCRIPTION

The HDAC754A is a monolithic, low cost, multiplying 12-bit digital-to-analog converter (DAC) designed for direct microprocessor interface. It is compatible with the industry standard 7545 but has significant performance improvements in speed and gain accuracy. The HDAC7545A is fabricated in a three-micron, polysilicon gate BEMOS process and operates from a single +5 V (maximum) supply. Excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is ensured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes for latch-up protection.

The HDAC7545A incorporates a parallel loading architecture for the DAC conversion bits. When pins $\overline{CS}$ and $\overline{WR}$ are low, the 12 input data registers read the bus data. The single load and convert operation allows one-cycle updating by 16-bit microprocessors.

With direct parallel bus data loading, the HDAC7545A is ideally suited for microprocessor-based instruments and industrial or process controllers.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
V_{DD} to GND ....+7 V
AGND to GND ....-0.3 to V_{DD}
Input Voltages
$V_{Rfeedback}$ to GND ....±25 V
Digital Input Voltage to GND ....0.3 to V_{DD}
Outputs
V_{out1} to GND ....-0.3 V to V_{DD}

Temperature
Operating Temperature, ambient............... -55 to +125 °C
junction......................... +150 °C
Lead Temperature, (soldering 10 seconds)........ +300 °C
Storage Temperature................................ -65 to +150 °C
Power Dissipation (Any Package) to +75 °C........ 450mW
(Derates above +75 °C by 6 mW/°C)

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal appliied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7545AA/G MIN	NOM	MAX	HDAC7545AA MIN	NOM	MAX	HDAC7545AB MIN	NOM	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		I		12			12			12		Bits
Relative Accuracy		I	-.5	±.25	+.5	-.5		+.5	-1		+1	LSB
Differential Nonlinearity		I	-.5	±.25	+.5	-.5		+.5	-1		+1	LSB
Gain Error	25 °C	I	-.5		+.5	-2		+2	-3		+3	LSB
Using Internal $R_{feedback}$	Tmin - Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Gain Temperature Coefficient		IV		0.3	3		0.3	3		0.3	3	ppm/°C
Output Leakage OUT1[4]												
	25 °C	I	-5		+5	-5		+5	-5		+5	nA
	0-70 °C/-25 to +85 °C	I	-10		+10	-10		+10	-10		+10	nA
	-55 to +125 °C	I	-100		+100	-100		+100	-100		+100	nA
	All digital inputs at 0 V											
Reference Input Resistance	Pin 19 to GND											
	+25 °C	IV	7	12.5	18	7	12.5	18	7	12.5	18	kΩ
	Temp. Coefficient	IV		-180			-180			-180		ppm/°C
DIGITAL INPUTS												
V_{IH} (High Input Voltage)		I	2.4			2.4			2.4			V
V_{IL} (Low Input Voltage)		I			0.8			0.8			0.8	V
I_{IN} (Input Currents I_{IH}, I_{IL})		I		±.005	±1		±.005	±1		±.005	±1	µA
C_{IN} (Input Capacitance)	VIN=0 Volts	IV			5			5			5	pF

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, $V_{DD}=+5$ V; $V_{REF}=+10$ V, OUT1=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7545AA/G MIN	NOM	MAX	HDAC7545AA MIN	NOM	MAX	HDAC7545AB MIN	NOM	MAX	UNITS
I_{DD}	Logic Inputs at V_{IL} or V_{IH}	I			4			4			4	mA
I_{DD}	25 °C Logic Inputs at 0 V or V_{DD}	I		10	100		10	100		10	100	µA
	T_{MIN} to T_{MAX}	I			500			500			500	µA
AC ELECTRICAL CHARACTERISTICS												
Propagation Delay[5]		IV		50	100		50	100		50	100	ns
Digital to Analog Glitch Impulse[1]	V_{REF}=AGND	IV		200	400		200	400		200	400	nV-sec
Multiplying Feedthrough Error	V_{REF} to V_{OUT} $V_{REF}=\pm10$ V 10 kHz Sinewave	IV		0.3	0.5		0.3	0.5		0.3	0.5	mV(p-p)
Output Current Settling Time[1,3]		IV		0.5	1.0		0.5	1.0		0.5	1.0	µsec
Capacitance OUT1	Digital Inputs=V_{IH} $\overline{WR}=\overline{CS}$=0 V	IV			75			75			75	pF
Capacitance OUT2	Digital Inputs=V_{IL} $\overline{WR}=\overline{CS}$=0 V	IV			30			30			30	pF
t_{CS} (Chip select set-up time)		I	60			60			60			ns
t_{CH} (Chip select hold time)		I	0			0			0			ns
t_{WR} (pulse width)	$t_{CS}\geq t_{WR}$	I	100			100			100			ns
t_{DS} (Data set-up time)		I	50			50			50			ns
t_{DH} (Data hold time)		I	9			9			9			ns

Note 1: OUT1 load: 100 Ω + 13 pF
Note 2: Digital inputs change from 0 V to V_{DD} or V_{DD} to 0 V
Note 3: Measured from falling edge of $\overline{WR}$.
Note 4: Digital inputs $\overline{WR}$ and $\overline{CS}$ at 0 V.
Note 5: Measured from falling edge of $\overline{WR}$ to 90% of final output value.

TEST LEVEL CODES

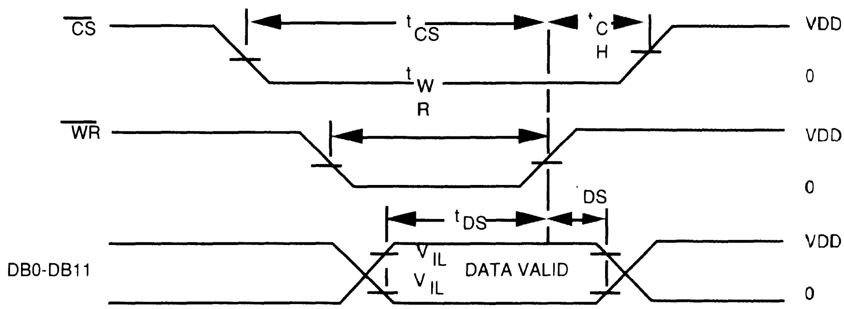
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Figure 1 - Write Cycle Timing Diagram



MODE SELECTION FOR FIGURE 1

WRITE MODE: $\overline{CS}$ and $\overline{WR}$ low. DAC responds to data inputs DB0-DB11.

HOLD MODE: $\overline{CS}$ and $\overline{WR}$ high. Data inputs DB0-DB11 are locked out; DAC holds last data present when $\overline{CS}$ or $\overline{WR}$ assumes high state.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in percentage of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7545A ideal full-scale output is -(4095)/(4096)•(V_{REF}). Gain error is adjustable to zero using external trims as shown in figures 6 and 7 and in Table 1.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the V_{REF} terminal to OUT1 with the DAC loaded to all 0s.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

PROPAGATION DELAY

This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE

This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV-secs and is measured with V_{REF}=GND.

CIRCUIT DESCRIPTION

As shown in the block diagram, the HDAC7545A consists of a 12 bit multiplying DAC and a 12 bit data latch. Data at pins DB0 - DB11 are latched when both pins $\overline{CS}$ and $\overline{WR}$ are low. Current latched data establishes the digital-to-analog conversion code, therefore, conversion is actually controlled by pins $\overline{CS}$ and $\overline{WR}$. This is described further in the Interface Logic section.

Figure 2A shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7545A uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7545A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the remaining VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switches route the bit-weighted current of the leg to either analog ground or to the output (pin OUT1). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the three most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7545A is identical to similar devices that use an unmodified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the external resistor shown in Figure 2A in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered VOUT, and in combination with the feedback resistance maintains OUT1 at virtual ground. The transfer function of Figure 2B shows the relationship of VOUT for an equivalent R-2R resistor network, shown in the same figure. A more detailed explanation of the circuit operation and performance aspects is found in the following Equivalent Circuit Analysis section.

Figure 2A - Simplified Circuit Description

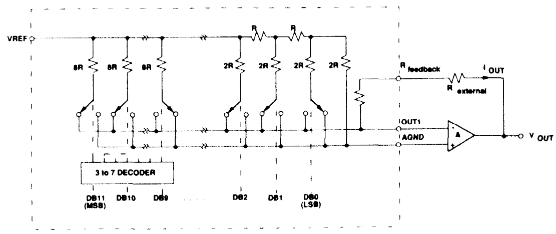
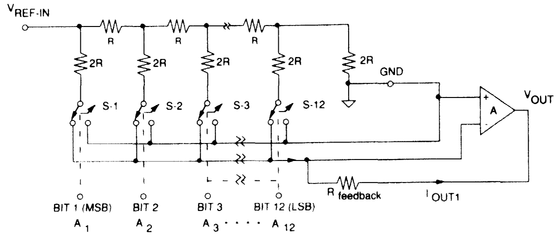


Figure 2B - Equivalent R-2R Network



The transfer function for the HDAC7545A connected in the multiplying mode as shown in figure 2B is:

$$V_O = V_{IN} \times \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} \bullet\bullet\bullet \frac{A_{12}}{2^{12}} \right)$$

in which A_x assumes a value of 1 for a HIGH bit and 0 for a Low bit.

EQUIVALENT CIRCUIT ANALYSIS

The equivalent output circuit of the HDAC7545A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects.

In figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to OUT2. OUT2 is internally connected to AGND in packaged versions of the HDAC7545A. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin V_{REF} plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in figures 3 and 4.

Figure 3 - HDAC7545A DAC Equivalent Circuit All Digital Inputs Low

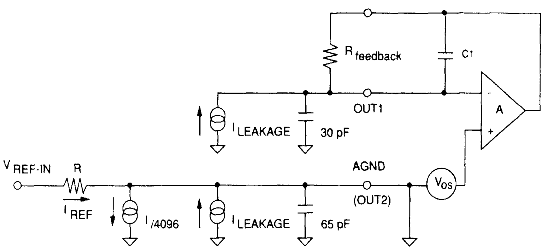
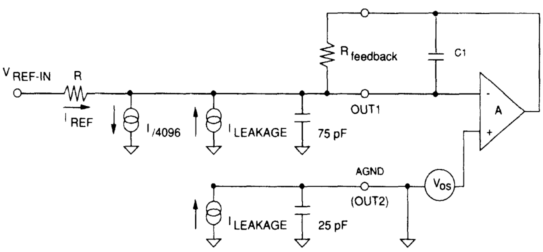


Figure 4 - HDAC7545A DAC Equivalent Circuit All Digital Inputs High



The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between figures 3 and 4, resistance at each op-amp input can change from 10k Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below:

Offset gain=1 + $R_{feedback}$/RDAC

With all code bits LOW:
RDAC >> $R_{feedback}$; offset gain=1

With all code bits HIGH:
RDAC= $R_{feedback}$; offset gain=2

Thus, the offset is not amplified by a constant gain over the range of code input. This variation in offset gain is seen as a nonlinearity in the voltage output over the full scale output. The magnitude of nonlinearity is the difference in the gains at code extremes times the offset voltage. In this DAC, this nonlinearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (figures 6 and 7). Although all R-2R DAC's have the need for this type of compensation, the HDAC7545A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7545A.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp: as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{OUT1} + C1}$.

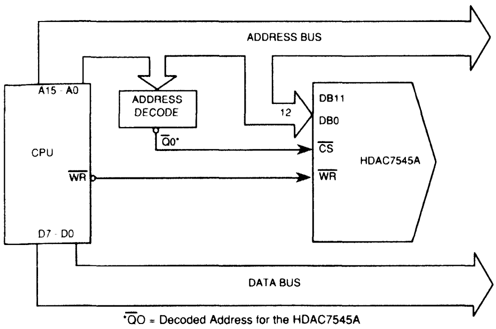
For an OP-27 used as an output op-amp with 8 MHz gain-bandwidth, the choice of C1 is:

$(2 \cdot \pi \cdot C1 \cdot R_{feedback})^{-1}$= 4 MHz or C1= 4 pf

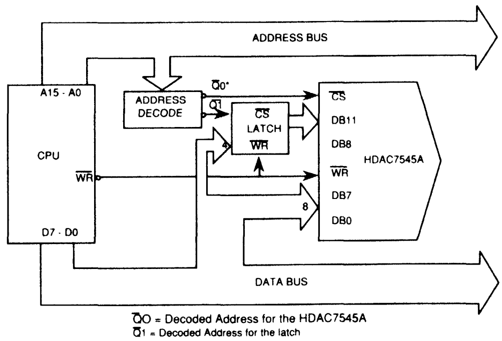
•$R_{feedback}$; offset gain =2

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7545A 's low output capacitance comes much closer to fulfilling this goal than most other 7545 compatible DAC's. Thus, faster, more well controlled settling is seen with the HDAC7545A.

Figure 5 - Typical Microprocessor Bus Interfaces



MULTIPLEXED BUS ARCHITECTURE



SEPARATE ADDRESS/DATA BUS ARCHITECTURE

INTERFACE LOGIC

The HDAC7545A is designed to allow control of the output via a parallel microprocessor bus I/O. This section describes operation of the intrface controls to accomplish this.

A typical parallel bus I/O configuration is shown in figure 5. The microprocessor provides the DAC code as well as all control signals to load the code and update the analog output. During loading, the HDAC7545A accepts the DAC input code in a 12-bit word.

When the $\overline{CS}$ pin is a logic 0, the input register of the HDAC7545A is enabled. The $\overline{WR}$ input actually strobes the input data from the paralled bus into the HDAC7545A data register. This occurs on the falling edge of this $\overline{WR}$ pulse. Figure 1, the Write Timing Diagram, defines the minimum set-up and hold times required by the control lines to successfully transfer data in this fashion.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

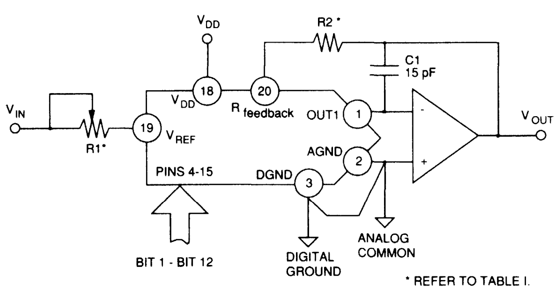
Figure 6 illustrates the use of the HDAC7545A in a unipolar (or 2 quadrant multiplication) mode. The V_{REF} is applied from pin 19 to ground voltage or an input current can be applied to pin 19. Positive or negative voltages/current can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the V_{REF} voltage out. If the source of V_{REF} is adjustable, V_{REF} could be directly adjusted for full scale calibration. (See Table II.)

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

The op-amp used with the HDAC7545A should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the offset effect which is code dependent and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

Figure 6 - Unipolar Binary Operation



BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7545A in a bipolar (or 4 quadrant multiplication) mode is illustrated in figure 7. The V_{REF} is applied from pin 17 to ground voltage or an input current can be applied to pin 17. Positive or negative voltages/current can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of V_{REF} to produce a maximum output which is half of V_{REF} in either polarity (see Table III for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the V_{REF} source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track each other for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate the OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

Table I - Recommended Trim Resistor Values vs Grades

TRIM RESISTOR	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

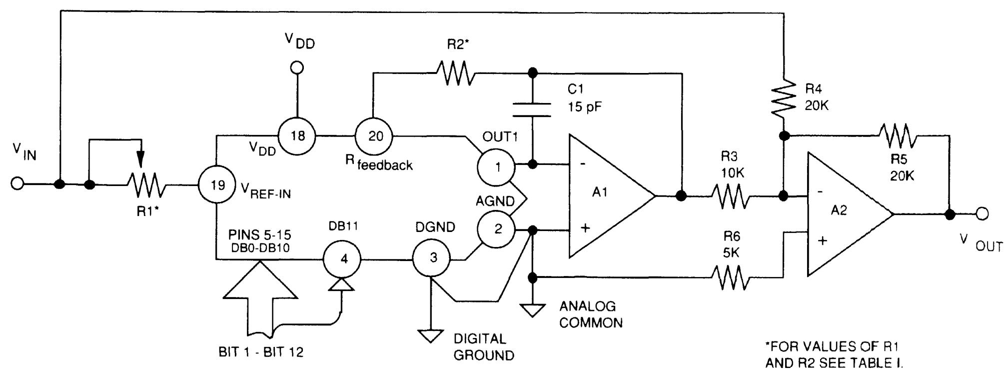
Table II - Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

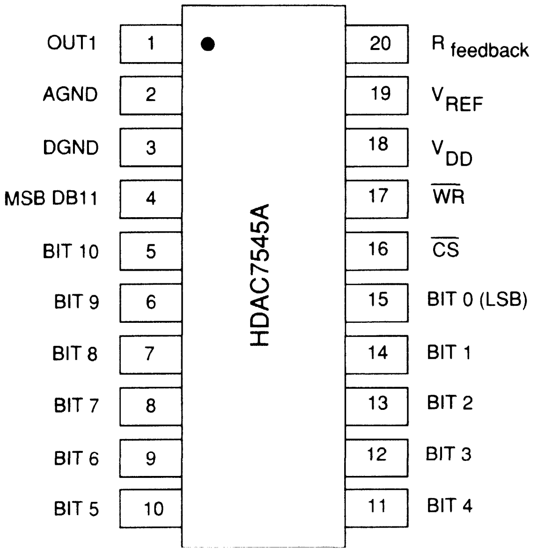
Table III - Bipolar Binary Code Table for Circuit of Figure 5

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Figure 7 - Bipolar Operation



PIN ASSIGNMENT HDAC7545A



PIN FUNCTIONS HDAC7545A

NAME	FUNCTION
OUT1	Analog Current Output
AGND	Analog Ground
DGND	Digital Logic Ground
DB11	Input Data Bit 11 (MSB)
DB10	Input Data Bit 10
DB9	Input Data Bit 9
DB8	Input Data Bit 8
DB7	Input Data Bit 7
DB6	Input Data Bit 6
DB5	Input Data Bit 5
DB4	Input Data Bit 4
DB3	Input Data Bit 3
DB2	Input Data Bit 2
DB1	Input Data Bit 1
DB0	Input Data Bit 0 (LSB)
$\overline{CS}$	Chip Select
$\overline{WR}$	Data Write
VDD	Positive Power Supply
VREF	Reference Input Voltage
$R_{feedback}$	Internal Feedback Resistor

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

HDAC10180

8-BIT, HIGH SPEED D/A CONVERTER

FEATURES

- 275 MWPS Conversion Rate - A Version
- 165 MWPS Conversion Rate - B Version
- Compatible with TDC1018 with Improved Performance
- RS-323-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10 kHz, 100 kΩ ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs

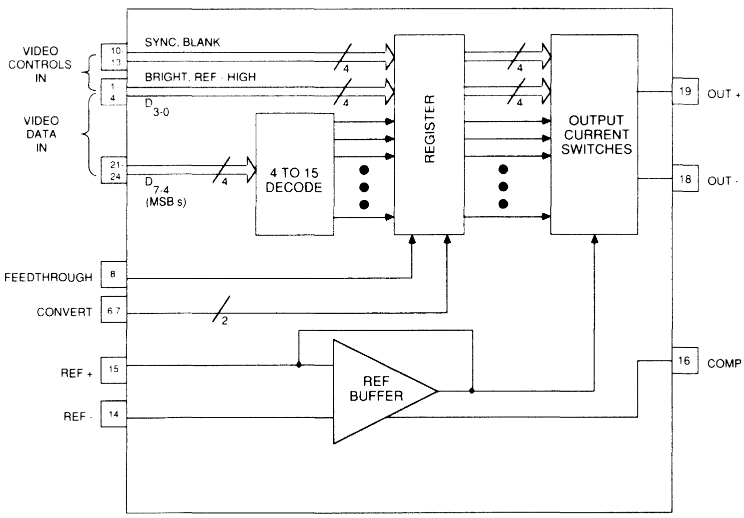
APPLICATIONS

- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The HDAC10180 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC10180 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC10180 is pin-compatible with the TDC1018, with improved performance, and two can be used with the HDAC10181. The HDAC10180 contains data and control input registers, video control logic, reference buffer, and current switches in a 24-lead CERDIP package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) ....-7.0 to 0.5 V
V_{EEA} (measured to V_{CCA}) ....-7.0 to 0.5 V
V_{CCA} (measured to V_{CCD}) ....-0.5 to 0.5 V

Input Voltages

CONV, Data, and Controls ....V_{EED} to 0.5 V
(measured to V_{CCD})

REF + (measured to V_{CCA}) ....V_{EEA} to 0.5 V
REF - (measured to V_{CCA}) ....V_{EEA} to 0.5 V

Temperature

Operating, ambient ....-55 to + 125 °C
junction ....+ 175 °C
Lead, Soldering (10 seconds) ....+ 300 °C
Storage ....-60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

V_{CCA} = 0.0 V, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A =T_{MIN} to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		I	-5		+5	% Full Scale
Gain Error Tempco		V		150		PPM/°C
Input Capacitance, REF +, REF -		V		5		pF
Compliance Voltage, + Output		I	-1.2		1.5	V
Compliance Voltage, - Output		I	-1.2		1.5	V
Equivalent Output Resistance		I	20			K Ohm
Output Capacitance		V		12		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		I			0.5	LSB
Input Voltage, Logic HIGH		I	-1.0			V
Input Voltage, Logic LOW		I			-1.5	V
Convert Voltage, Common Mode Range		I	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		I			120	µA
Input Current, Logic HIGH, Data and Controls		I		10	120	µA
Input Current, Convert		I		2	60	µA

ELECTRICAL SPECIFICATIONS

V_{CCA} = 0.0 V, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Capacitance, Data and Controls		V		3		pF
Power Supply Sensitivity		I	-120		+120	µA/V
Supply Current		I		175	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 Ohms, C_L = 5 pF, T_A = 25 °C, I_{SET} = 1.105 mA)						
Maximum Conversion Rate	B Grade A Grade	III III	165 275			MWPS MWPS
Rise Time	10% to 90% G.S.	III			1.6	ns
Rise Time	10% to 90% G.S. R_L = 25 Ohms	IV		1.0		ns
Current Settling Time, Clocked Mode	To 0.2%	IV		7		ns
Current Settling Time, Clocked Mode	To 0.8%	IV		5.5		ns
Current Settling Time, Clocked Mode	To 0.2% R_L = 25 Ω	IV		4.5		ns
Clock to Output Delay, Clocked Mode		III			4	ns
Data and Output Delay, Transparent Mode		III			6	ns
Convert Pulse Width, (LOW or HIGH)	B Grade A Grade	III III	3.0 1.8			ns ns
Glitch Energy	Area = 1/2 VT	V		10		pV-s
Reference Bandwidth, -3 dB		V		1		MHz
Set-up Time, Data and Controls		III	1.3	1.8	2	ns
Hold Time, Data and Controls		III	0.5	0		ns
Slew Rate	20% to 80% G.S.	III	400			V/µS
Clock Feedthrough		III			-48	dB

TEST LEVEL CODES

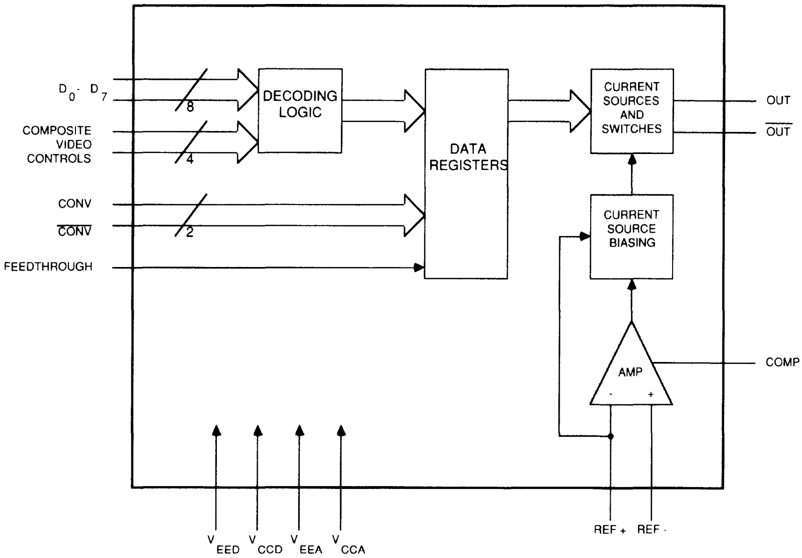
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

FUNCTIONAL DIAGRAM



APPLICATION INFORMATION

The HDAC10180 is a high speed video Digital-to-Analog converter capable of up to 275 MWPS conversion rates. This makes the device suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates.

The HDAC10180 is separated into different conversion rate categories as shown in Table I.

The HDAC10180 has 10 KH and 100K ECL logic level compatible video controls and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC10180 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

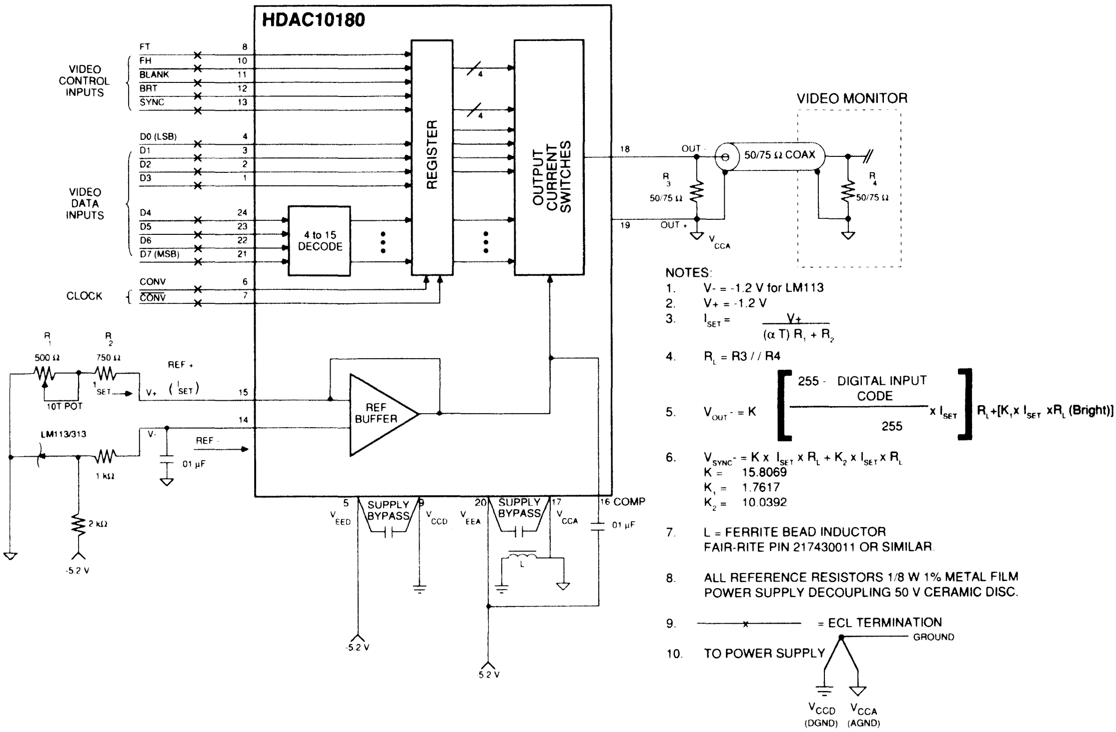
The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered VIDEO DACs.

Table I - The HDAC10180 Family and Speed Designations

PART NUMBER	UPDATE	COMMENTS
HDAC10180A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
HDAC10180B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

Figure 1 - Typical Interface Circuit



TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC10180 in a color raster application is shown in Figure 1. The HDAC10180 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC10180 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC10180. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a -2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC10180 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC10180 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The HDAC10180 operates from a single standard -5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC10180's inherent supply noise rejection characteristics. As shown in Figure 1, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC10180 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC10180 has two reference inputs: REF - and REF +. Both pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 7.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the REF + input on the HDAC10180. A method and equations to set I_{SET} is shown in Figure 1. The HDAC10180 uses an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the REF - pin should be driven through a resistor to minimize offsets caused by bias current. The value for I_{SET} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased 50% more than ISET for doubly terminated 75 Ohm video applications.

COMPENSATION

The HDAC10180 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor (C_C) should be connected between COMP and V_{EEA} as shown in Figure 1. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, the C_C should be large (.01 µF). The value of C_C determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of C_C can be used to get up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The HDAC10180 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC10180 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 2).

Figure 2 - Timing Diagram

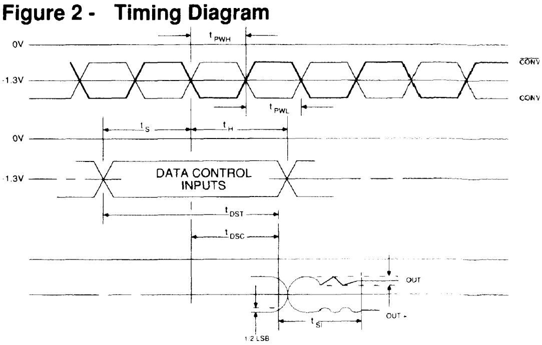


Table II - Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table II shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 8).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC10180. Since the actual switching threshold of $\overline{\text{CONV}}$ is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC10180 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{REF} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 4, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The OUT - output (Figure 8) will provide a video output waveform with the SYNC pulse bottom at the -1.07 V level. The OUT + is inverted with SYNC up.

Figure 3 - CONVert, $\overline{\text{CONVert}}$ Switching Levels

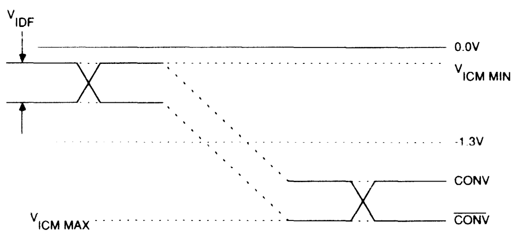


Figure 4A - Standard Load

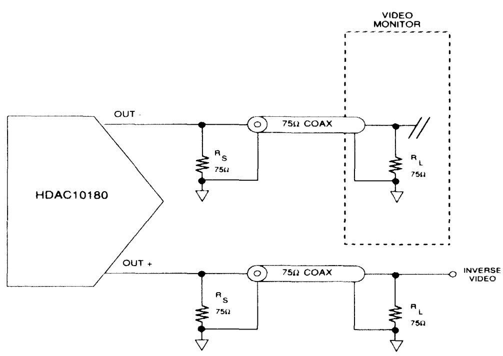
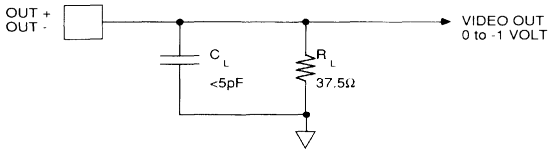


Figure 4B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC10181 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 µA to an external load, such as two other DAC reference inputs. (See HDAC10181 Data Sheet).

The circuits shown in Figure 5 illustrate how a single HDAC10181 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC10181's reference output. The HDAC10180s shown are especially well-suited to be slaved to a 10181 for a better TC tracking from DAC-to-DAC, since they are essentially 10181s without the reference. The 10180 is pin-compatible with the TDC1018, which does not have an internal reference. Although either the TDC1018 or HDAC10180 may be slaved from an HDAC10181, the higher performance HDAC10180 and the above mentioned DAC-to-DAC TC tracking is the best choice for new designs.

No external reference is required for operation of the HDAC10181, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The HDAC10180 must use an external reference.

Figure 5 - Typical RGB Graphics System

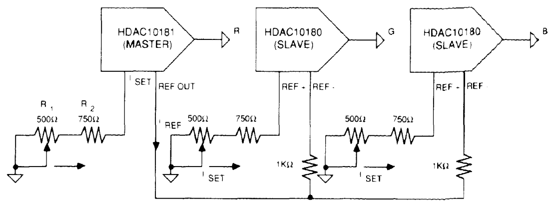


Figure 6 - Burn-In Circuit

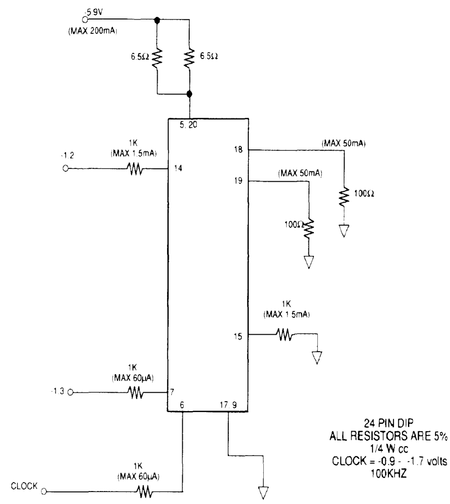


Figure 7 - DAC Output Circuit

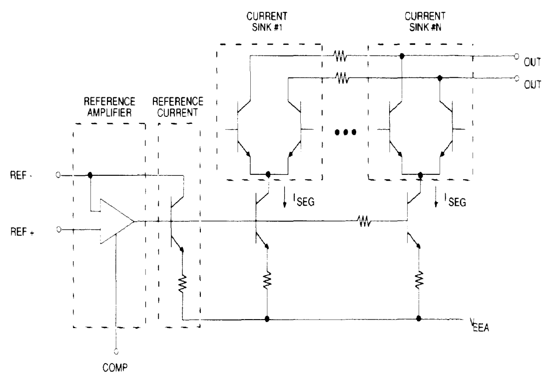


Figure 8 - Video Output Waveform for Standard Load

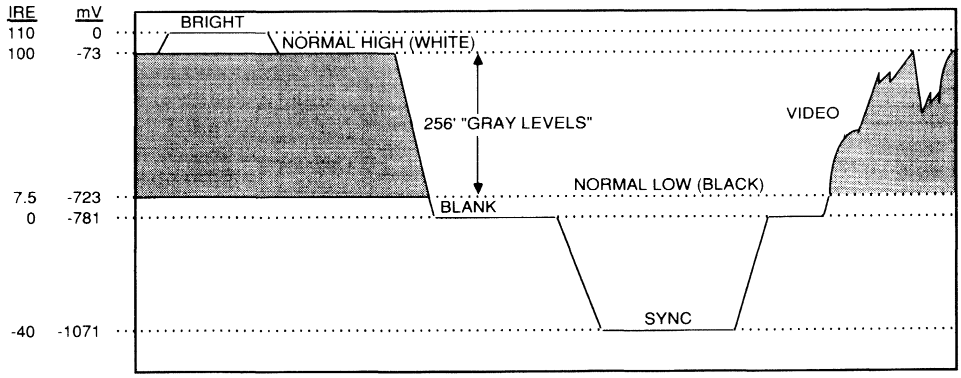
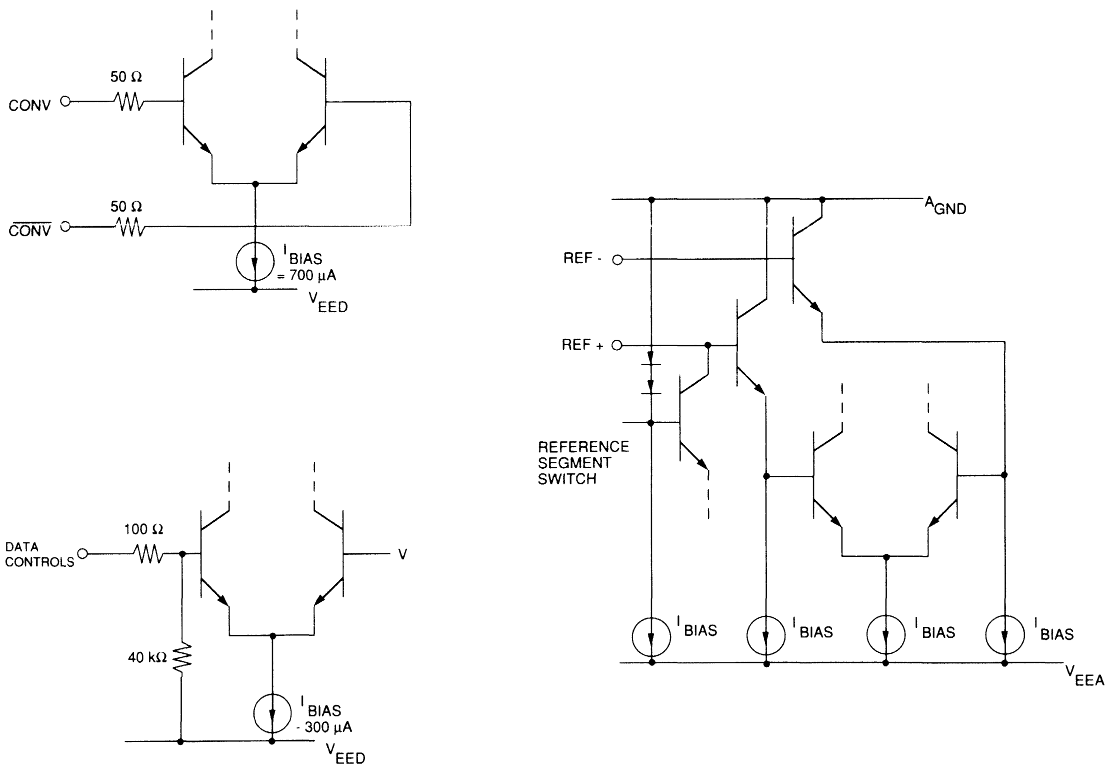
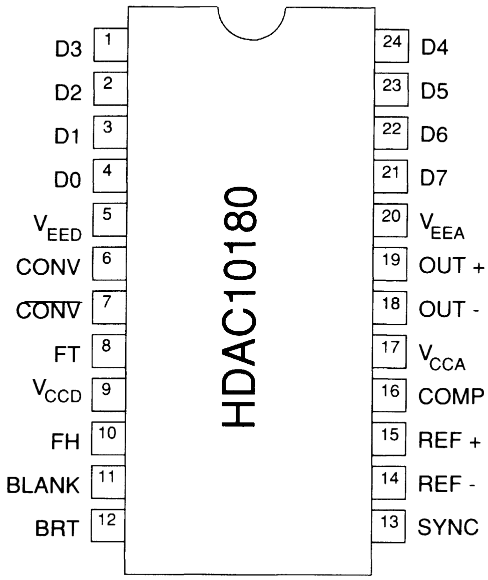


Figure 9 - Equivalent Input Circuits - Data, Clock, Controls and Reference



PIN ASSIGNMENTS



24 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
V_{EED}	Digital Negative Supply
CONV	Convert Clock Input
$\overline{CONV}$	Convert Clock Input Complement
FT	Register Feedthrough Control
V_{CCD}	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF -	Reference Current - Input
REF +	Reference Current + Input
COMP	Compensation Input
V_{CCA}	Analog Positive Supply
OUT -	Output Current Negative
OUT +	Output Current Positive
V_{EEA}	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

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4

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

HDAC10181

8-BIT, HIGH SPEED D/A CONVERTER

SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- 275 MWPS Conversion Rate - A Version
- 165 MWPS Conversion Rate - B Version
- RS-323-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10 KH, 100 kΩ ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs
- Stable On-Chip Bandgap Reference

APPLICATIONS

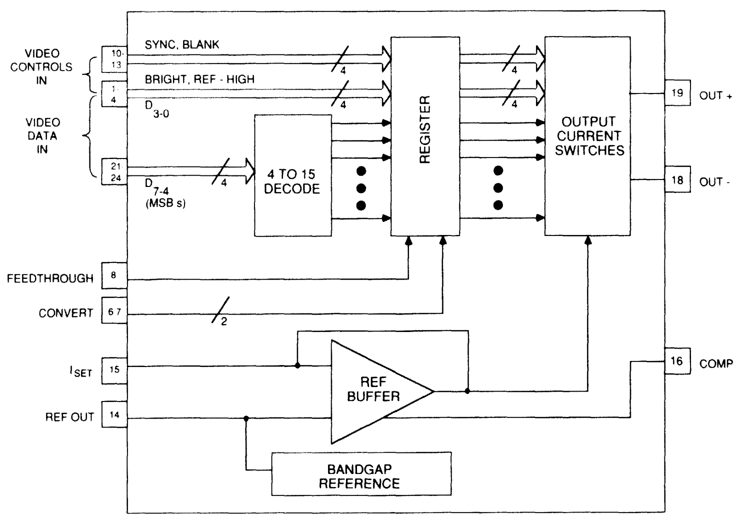
- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

4

GENERAL DESCRIPTION

The HDAC10181 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC10181 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC10181 includes an internal precision bandgap reference which can drive two HDAC10180s in an RGB graphics system. The HDAC10181 contains data and control input registers, video control logic, reference buffer, and current switches in 24 Lead CERDIP package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which the useful life will be impaired)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) ....-7.0 to 0.5 V
V_{EEA} (measured to V_{CCA}) ....-7.0 to 0.5 V
V_{CCA} (measured to V_{CCD}) ....-0.5 to 0.5 V

Input Voltages

CONV, Data, and Controls .... V_{EED} to 0.5 V
(measured to V_{CCD})

I_{SET} (measured to V_{CCA}) .... V_{EEA} to 0.5 V
REF OUT (measured to V_{CCA}) .... V_{EEA} to 0.5 V

Temperature

Operating, ambient ....-60 to + 140 °C
junction ....+ 175 °C
Lead, Soldering (10 seconds) ....+ 300 °C
Storage ....-60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

V_{CCA} = 0.0 V, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		I	-19		+19	% Full Scale
Gain Error Tempco		V		250		PPM/°C
Input Capacitance, I_{SET}, REF OUT		V		5		pF
Compliance Voltage, + Output		I	-1.2		1.5	V
Compliance Voltage, - Output		I	-1.2		1.5	V
Equivalent Output Resistance		I	20			K Ohm
Output Capacitance		V		12		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		I			0.5	LSB
Input Voltage, Logic HIGH		I	-1.0			V
Input Voltage, Logic LOW		I			-1.5	V
Convert Voltage, Common Mode Range		I	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		I			120	µA
Input Current, Logic HIGH, Data and Controls		I		10	120	µA
Input Current, Convert		I		2	60	µA

ELECTRICAL SPECIFICATIONS

V_{CCA} = 0.0 V, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Capacitance, Data and Controls		V		3		pF
Power Supply Sensitivity		I	-120		+120	µA/V
Supply Current		I		175	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 Ohms, C_L = 5 pF)						
Maximum Conversion Rate	B Grade A Grade	III III	165 275			MWPS
Rise Time	10% to 90% G.S.	III			1.6	ns
Rise Time	10% to 90% G.S. R_L = 25 Ohms	IV		1.0		ns
Current Settling Time, Clocked Mode	To 0.2%	IV		7		ns
Current Settling Time, Clocked Mode	To 0.8%	IV		5.5		ns
Current Settling Time, Clocked Mode	To 0.2% R_L = 25 Ω	IV		4.5		ns
Clock to Output Delay, Clocked Mode		III			4	ns
Data and Output Delay, Transparent Mode		III			6	ns
Convert Pulse Width, LOW	B Grade A Grade	III III	3.0 1.8			ns
Glitch Energy	Area = 1/2 VT	V		10		pV-s
Convert Pulse Width, HIGH	B Grade A Grade	III III	3.0 1.8			ns ns
Reference Bandwidth, -3 dB		V		1		MHz
Set-up Time, Data and Controls		III	1.3	1.8	2	ns
Hold Time, Data and Controls		III	0.5	0		ns
Slew Rate	20% to 80% G.S.	III	400			V/µS
Clock Feedthrough	.	III			-48	dB

TEST LEVEL CODES

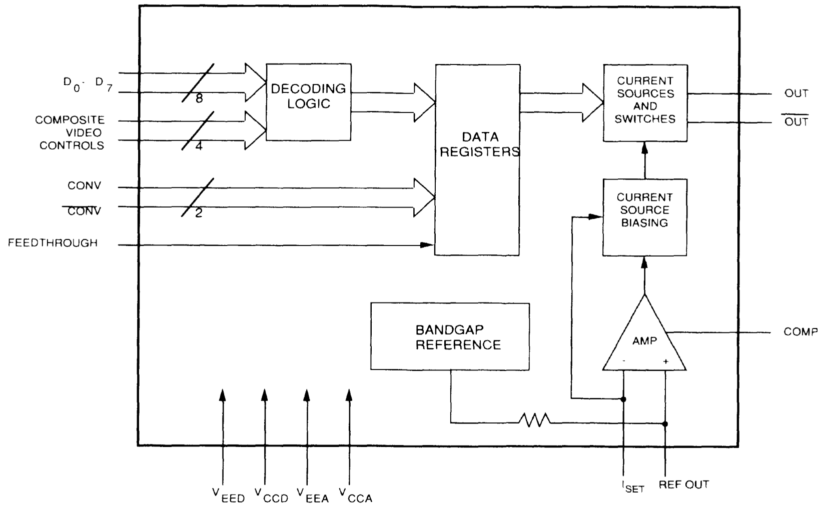
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

FUNCTIONAL DIAGRAM



APPLICATION INFORMATION

The HDAC10181 is a high speed video Digital-to-Analog converter capable of up to 275 MWPS conversion rates. This makes the devices suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates.

The HDAC10181 is separated into different conversion rate categories as shown in Table I.

The HDAC10181 has 10 KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC10181 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches. MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

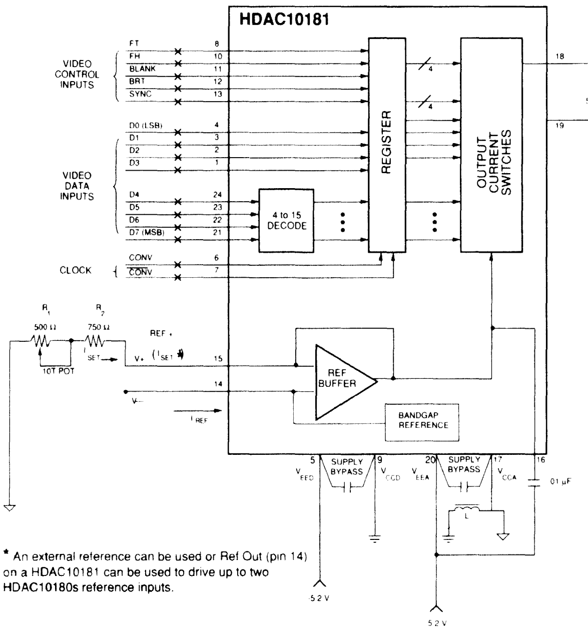
The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

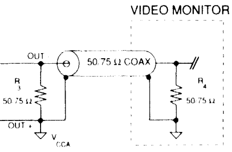
Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered VIDEO DACs.

Table I - The HDAC10181 Family and Speed Designations

PART NUMBER	UPDATE	COMMENTS
HDAC10181A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
HDAC10181B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

Figure 1 - Typical Interface Circuit





NOTES:

1. V- = -1.2 V (typical)
2. V+ = -1.2 V
3. $I_{SET} = \frac{V+}{\alpha T(R_1 + R_2)}$; typ = -1.105 mA
4. R_L = R3 // R4
5. $V_{OUT-} = K \frac{255 - \text{DIGITAL INPUT CODE}}{255} \times I_{SET} R_L + [K_1 \times I_{SET} \times R_L (\text{Bright})]$
6. $V_{SYNC-} = (K \times I_{SET} \times R_L) + (K_2 \times I_{SET} \times R_L)$

   K = 15.8069
   K_1 = 1.7617
   K_2 = 10.0392
7. L = Ferrite Bead Inductor Fair-rite Pin 217430011 Or Similar.
8. All Reference Resistors 1/8 W 1% Metal Film Power Supply Decoupling 50 V Ceramic Disc.
9. ——x—— = ECL Termination
10. To Power Supply

    GROUND
    V_{CCD} V_{CCA}
    (DGND) (AGND)

TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC10181 in a color raster application is shown in Figure 1. The HDAC10181 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC10181 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC10181. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a -2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC10181 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC10181 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The HDAC10181 operates from a single standard -5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC10181 inherent supply noise rejection characteristics. As shown in Figure 1, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC10181 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC10181 has one input (ISET) and one reference output (REF OUT). Both pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier. The HDAC10181 has a bandgap reference connected internally to the inverting output of the buffer amplifier and the REF OUT.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 6.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the I_{SET} input on the HDAC10181. A method and equations to set I_{SET} is shown in Figure 1. The HDAC10181 uses its own reference voltage for setting up I_{SET} as shown in Figure 1. The value for I_{SET} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased 50% more than I_{SET} for doubly terminated 75 Ohm video applications.

COMPENSATION

The HDAC10181 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor (C_C) should be connected between COMP and V_{EEA} as shown in Figure 1. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, the C_C should be large (.01 µF). The value of C_C determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of C_C can be used to get up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The HDAC10181 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC10181 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 2).

Figure 2 - Timing Diagram

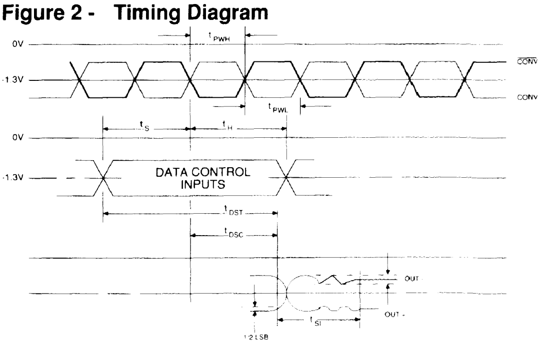


Table II - Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table II shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 8).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL drive, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC10181. Since the actual switching threshold of $\overline{\text{CONV}}$ is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC10181 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scales output can be changed by setting I_{REF} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 4, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The OUT - output (Figure 8) will provide a video output waveform with the SYNC pulse bottom at the -1.07 V level. The OUT + is inverted with SYNC up.

Figure 3 - CONVert, $\overline{\text{CONVert}}$ Switching Levels

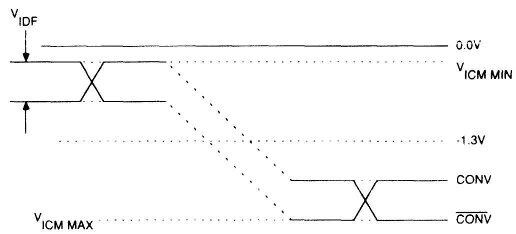


Figure 4A - Standard Load

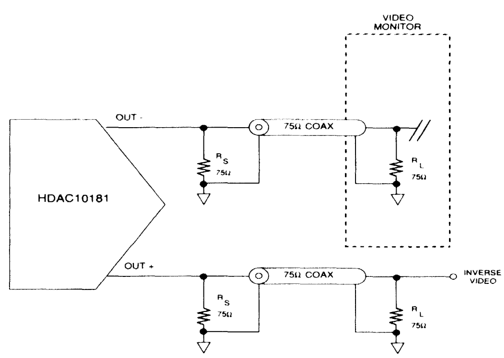
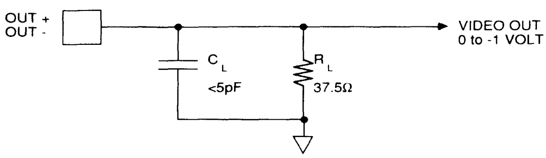


Figure 4B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC10181 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 μA to an external load, such as two other DAC reference inputs.

The circuits shown in Figure 5 illustrate how a single HDAC10181 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC10181's reference output. The HDAC10180s shown are especially well-suited to be slaved to a 10181 for a better TC tracking from DAC-to-DAC, since they are essentially 10181s without the reference. The 10180 is pin-compatible with the TDC1018, which does not have an internal reference. Although either the TDC1018 or HDAC10180 may be slaved from an HDAC10181, the higher performance HDAC10180 and the above mentioned DAC-to-DAC TC tracking is the best choice for new designs. (See 10180 data sheet.)

No external reference is required for operation of the HDAC10181, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The HDAC10180 must use an external reference.

Figure 5 - Typical RGB Graphics System

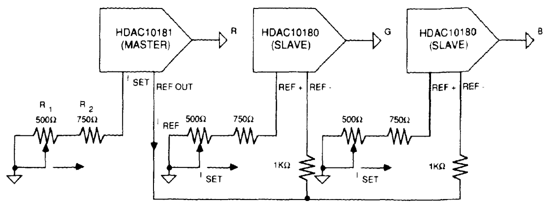


Figure 6 - Burn-In Circuit

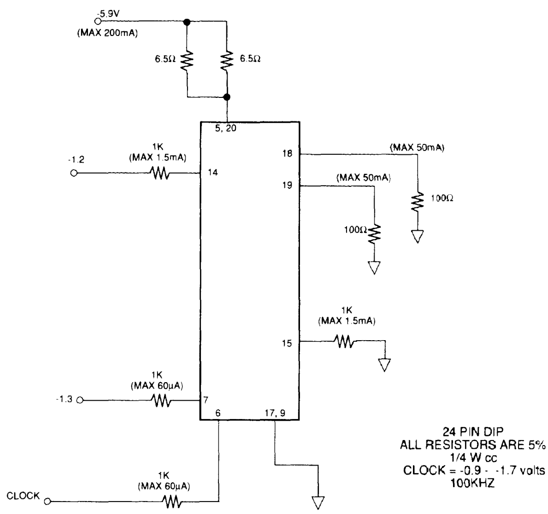


Figure 7 - DAC Output Circuit

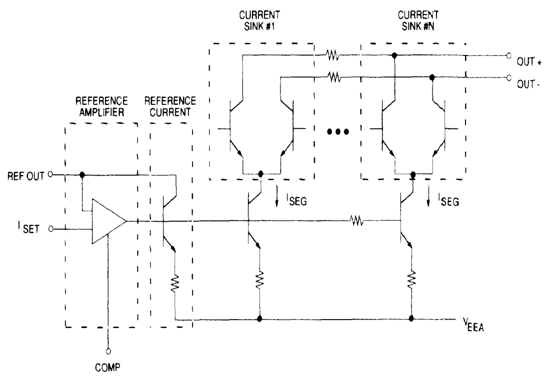


Figure 8 - Video Output Waveform for Standard Load

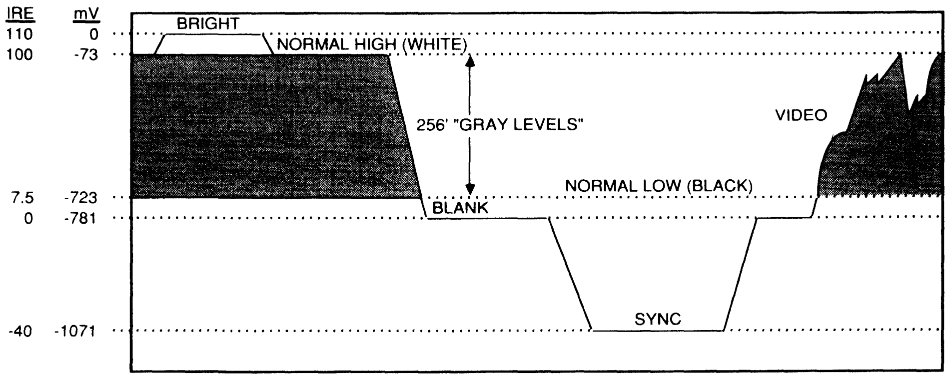
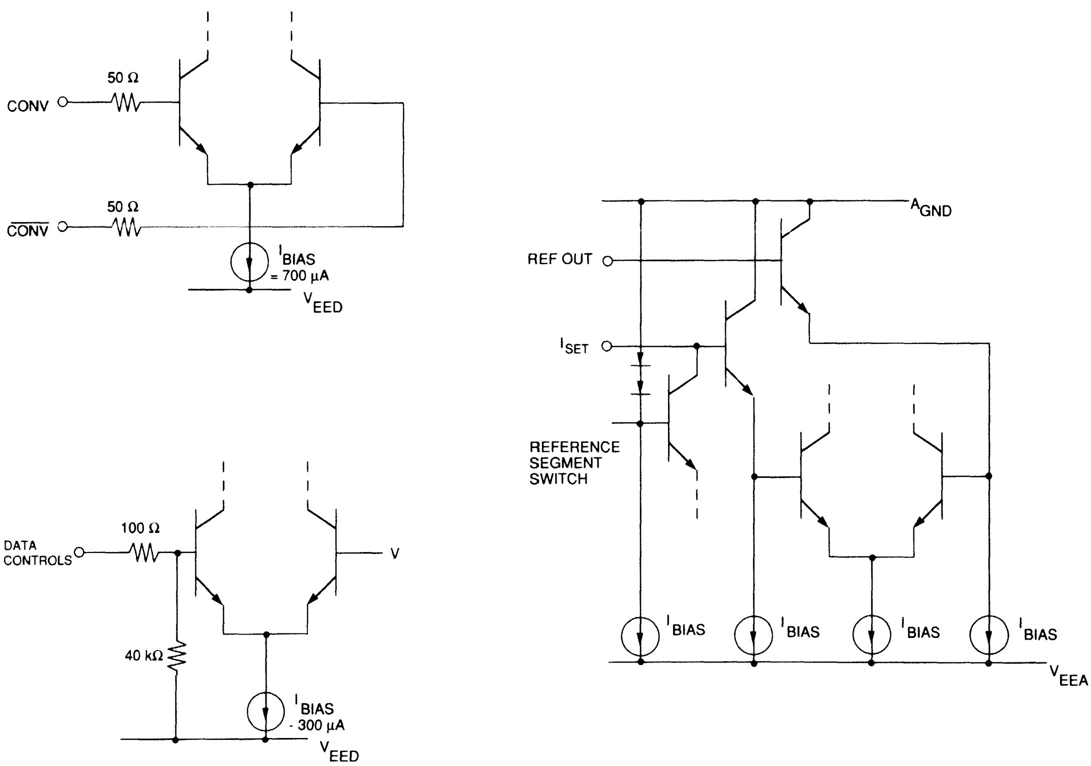
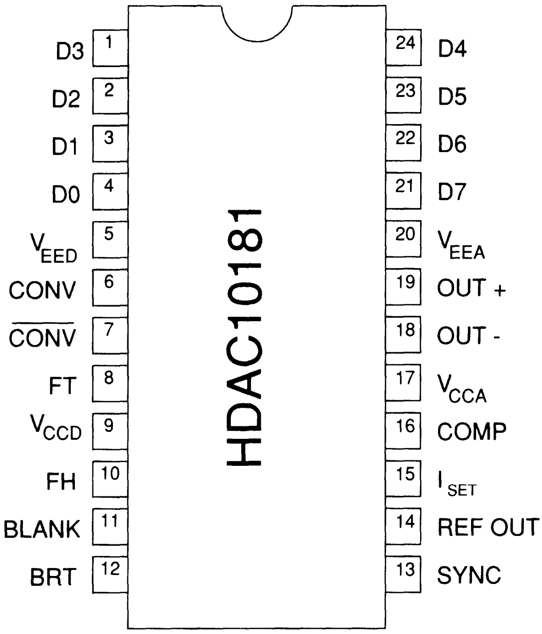


Figure 9 - Equivalent Input Circuits - Data, Clock, Controls and Reference



PIN ASSIGNMENTS



24 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
V_{EED}	Digital Negative Supply
CONV	Convert Clock Input
$\overline{CONV}$	Convert Clock Input Complement
FT	Register Feedthrough Control
V_{CCD}	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF OUT	Reference Output
I_{SET}	Reference Current + Input
COMP	Compensation Input
V_{CCA}	Analog Positive Supply
OUT -	Output Current Negative
OUT +	Output Current Positive
V_{EEA}	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

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SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

HDAC51400

8-BIT, ULTRAHIGH SPEED D/A CONVERTER

FEATURES

- 400 MWPS Nominal Conversion Rate
- RS-323-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10 KH, 100K ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs
- Stable On-Chip Bandgap Reference
- 50 and 75 Ohm Output Drive

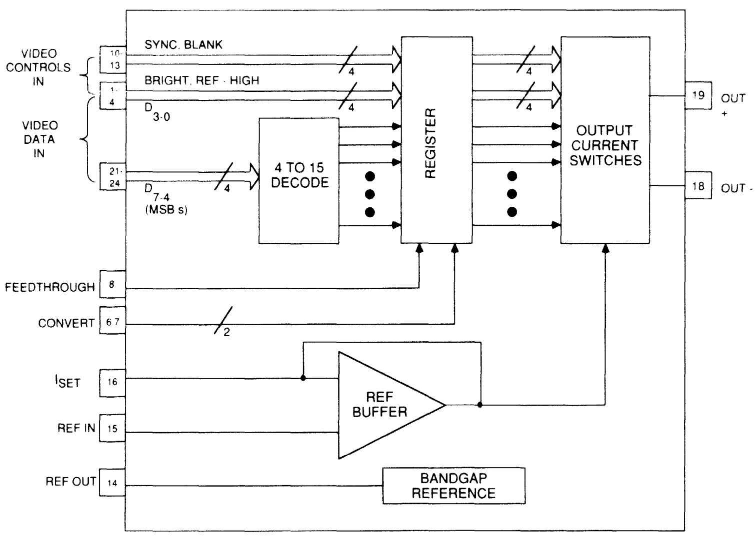
APPLICATIONS

- Raster Graphics
- High Resolution Color or Monochrome Displays to 2k x 2k Pixels
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The HDAC51400 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 400 MWPS. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC51400 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC51400 includes an internal precision bandgap reference which can drive two other HDAC51400s in an RGB graphics system. The HDAC51400 contains data and control input registers, video control logic, reference buffer, and current switches in a 24 Lead CERDIP package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which the useful life will be impaired)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) .... -7.0 to 0.5 V
V_{EEA} (measured to V_{CCA}) .... -7.0 to 0.5 V
V_{CCA} (measured to V_{CCD}) .... -0.5 to 0.5 V

Input Voltages

CONV, Data, and Controls .... V_{EED} to 0.5 V
(measured to V_{CCD})

REF+ (measured to V_{CCA}) .... V_{EEA} to 0.5 V
REF– (measured to V_{CCA}) .... V_{EEA} to 0.5 V

Temperature

Operating, ambient .... -55 to + 125 °C
junction .... + 175 °C
Lead, Soldering (10 seconds) .... + 300 °C
Storage .... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$V_{CCD}=V_{CCA}$ = 0.0 V, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		I	-5		+5	% Full Scale
Gain Error Tempco		IV		150		PPM/°C
Bandgap Tempco		IV		100		PPM/°C
Input Capacitance, I_{SET}, REF OUT		V		5		pF
Compliance Voltage, + Output		I	-1.2		1.5	V
Compliance Voltage, - Output		I	-1.2		1.5	V
Equivalent Output Resistance		I	20			kΩ
Output Capacitance		V		9		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		I			0.5	LSB
Input Voltage, Logic HIGH		I	-1.0			V
Input Voltage, Logic LOW		I			-1.5	V
Convert Voltage, Common Mode Range		I	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		I			120	µA
Input Current, Logic HIGH, Data and Controls		I		10	120	µA
Input Current, Convert		I		2	60	µA
Reference Voltage Measured to V_{CCA}		IV		-1.2		V
Reference Output Current		I	-50			µA

ELECTRICAL SPECIFICATIONS

V_{CCA} = 0.0 V, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Capacitance, Data and Controls		V		3		pF
Power Supply Sensitivity		I	-120		+120	µA/V
Supply Current		I		175	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 Ohms, C_L = 5 pF, T_A=+25 °C, I_{SET}=1.105 mA)						
Maximum Conversion Rate		IV	385	400		MWPS
Rise Time	10% to 90% G.S.	IV			900	ps
Rise Time	10% to 90% G.S. R_L = 25 Ohms	IV			600	ps
Current Settling Time, Clocked Mode	To 0.2% G.S.	IV		4		ns
Current Settling Time, Clocked Mode	To 0.2% R_L = 25 Ω	IV		3		ns
Clock to Output Delay, Clocked Mode		III			4	ns
Data and Output Delay, Transparent Mode		III			6	ns
Convert Pulse Width, LOW		IV		1.25		ns
Glitch Energy	Area = 1/2 VT	V		10		pV-s
Convert Pulse Width, HIGH		III		1.25		ns
Reference Bandwidth, -3 dB		V		1.25		MHz
Set-up Time, Data and Controls		III		1		ns
Hold Time, Data and Controls		III	0.	-200		ps
Slew Rate	20% to 80% G.S.	V		700		V/µS
Clock Feedthrough		III			-48	dB

TEST LEVEL CODES

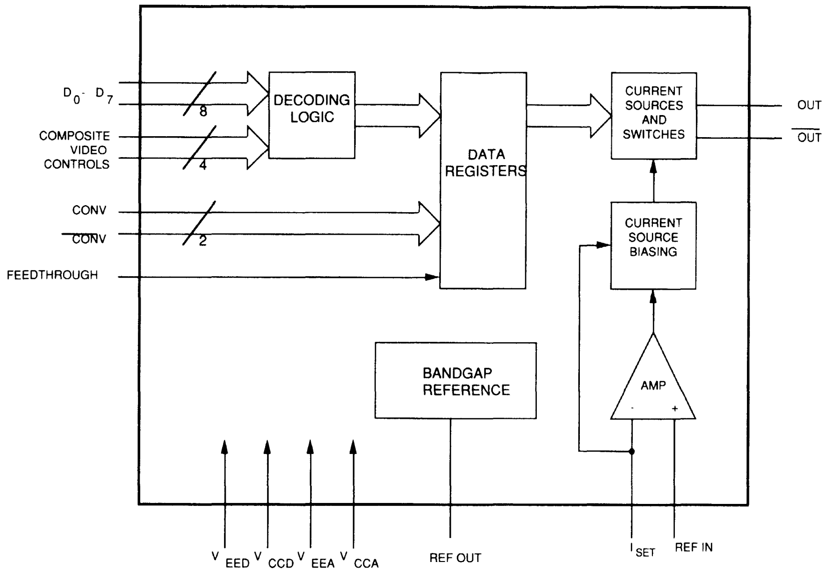
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

FUNCTIONAL DIAGRAM



APPLICATION INFORMATION

The HDAC51400 is a high speed video Digital-to-Analog converter capable of up to 400 MWPS conversion rates. This makes the devices suitable for driving 2048 X 2048 pixel displays at 60 to 90 Hz update rates.

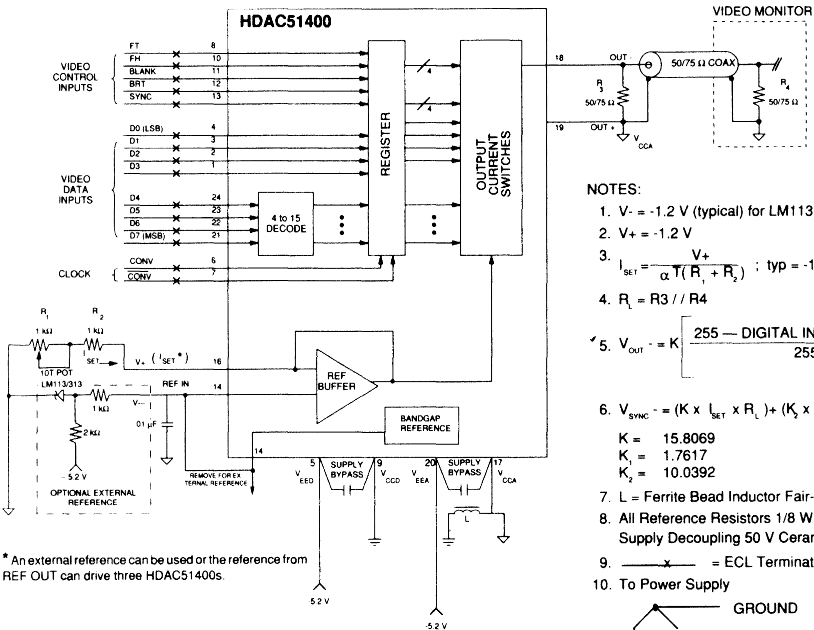
In addition, the HDAC51400 includes an internal bandgap reference which may be used to drive two other HDAC51400s if desired.

The HDAC51400 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC51400 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches. MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered VIDEO DACs.

Figure 1 - Typical Interface Circuit



* An external reference can be used or the reference from REF OUT can drive three HDAC51400s.

NOTES:

1. V- = -1.2 V (typical) for LM113 or V_{BG} (pin 14)
2. V+ = -1.2 V
3. $I_{SET} = \frac{V+}{\alpha T(R_1 + R_2)}$; typ = -1.105 mA
4. R_L = R3 / / R4
5. $V_{OUT}- = K\left[\frac{255 - \text{DIGITAL INPUT CODE}}{255} \times I_{SET}\right] R_L + [K_1 \times I_{SET} \times R_L (\text{Bright})]$
6. $V_{SYNC}- = (K \times I_{SET} \times R_L) + (K_2 \times I_{SET} \times R_L)$

   K = 15.8069
   K_1 = 1.7617
   K_2 = 10.0392
7. L = Ferrite Bead Inductor Fair-rite Pin 217430011 Or Similar.
8. All Reference Resistors 1/8 W 1% Metal Film Power Supply Decoupling 50 V Ceramic Disc.
9. ——x—— = ECL Termination
10. To Power Supply

GROUND

V_{CCD} V_{CCA}
(DGND) (AGND)

TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC51400 in a color raster application is shown in Figure 1. The HDAC51400 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC51400 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC51400. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a -2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC51400 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a doubly terminated 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC51400 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The HDAC51400 operates from a single standard -5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC51400 inherent supply noise rejection characteristics. As shown in Figure 1, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC51400 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC51400 has two reference inputs: REF IN and I_{SET}, and one reference output REF OUT. The input pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 7.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the (I_{SET}) input on the HDAC51400. A method and equations to set I_{SET} are shown in Figure 1. The HDAC51400 can use an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the REF IN in should be driven through a resistor to minimize offsets caused by bias current. The value for I_{SET} can be varied with the 500 to 1k Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased by 50% above for doubly-terminated 75 Ohm video applications.

DATA INPUTS AND VIDEO CONTROLS

The HDAC51400 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC51400 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_H after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 2).

Figure 2 - Timing Diagram

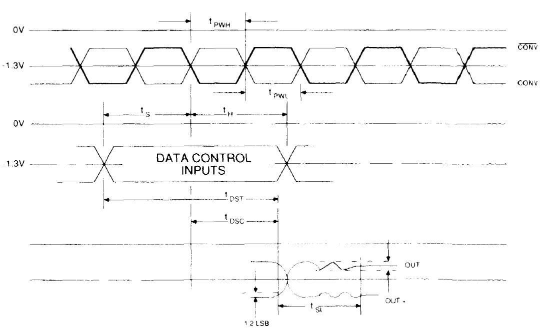


Table I - Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table I shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 8).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL drive, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC51400. Since the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC51400 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scales output can be changed by setting I_{SET} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 4, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The OUT - output (Figure 8) will provide a video output waveform with the SYNC pulse bottom at the -1.07 V level. The OUT + is inverted with SYNC up.

Figure 3 - CONVert, $\overline{\text{CONV}}$ert Switching Levels

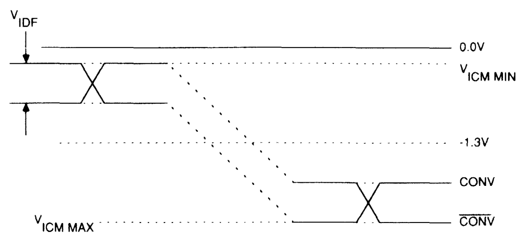


Figure 4A - Standard Load

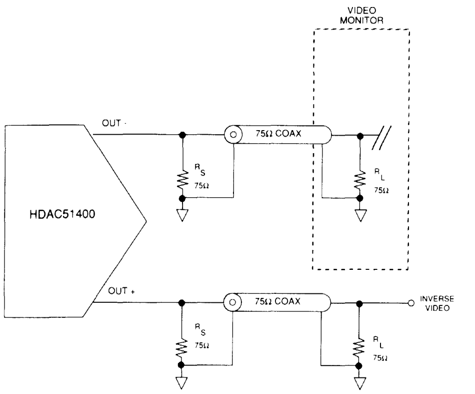
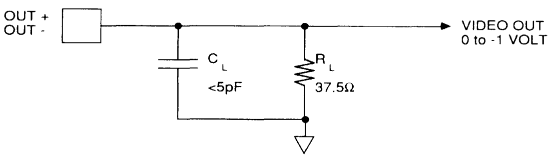


Figure 4B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC51400 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 µA to an external load, such as two other DAC reference inputs.

The circuits shown in Figure 5 illustrate how a single HDAC51400 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC51400's reference output.

Figure 5 - Typical RGB Graphics System

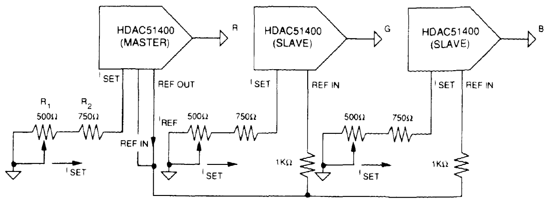


Figure 6 - Burn-In Circuit

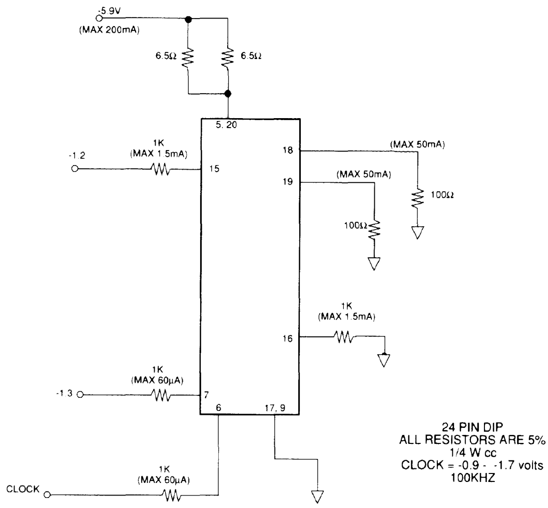
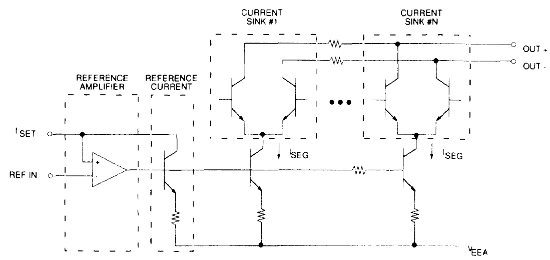


Figure 7 - DAC Output Circuit



SPT

Figure 8 - Video Output Waveform for Standard Load

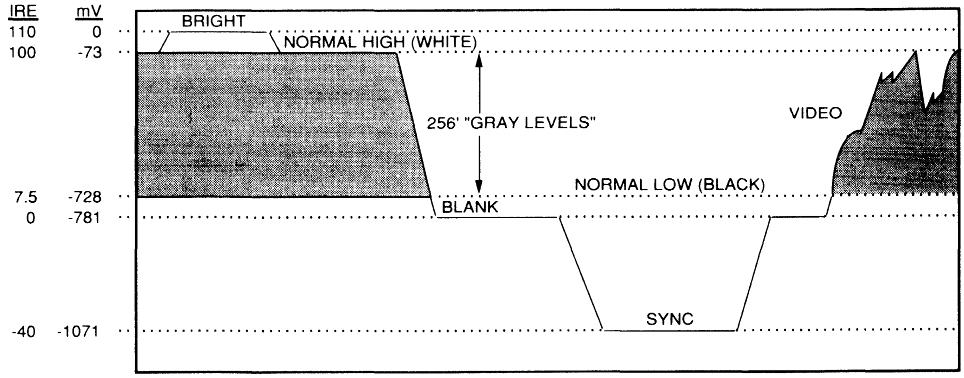
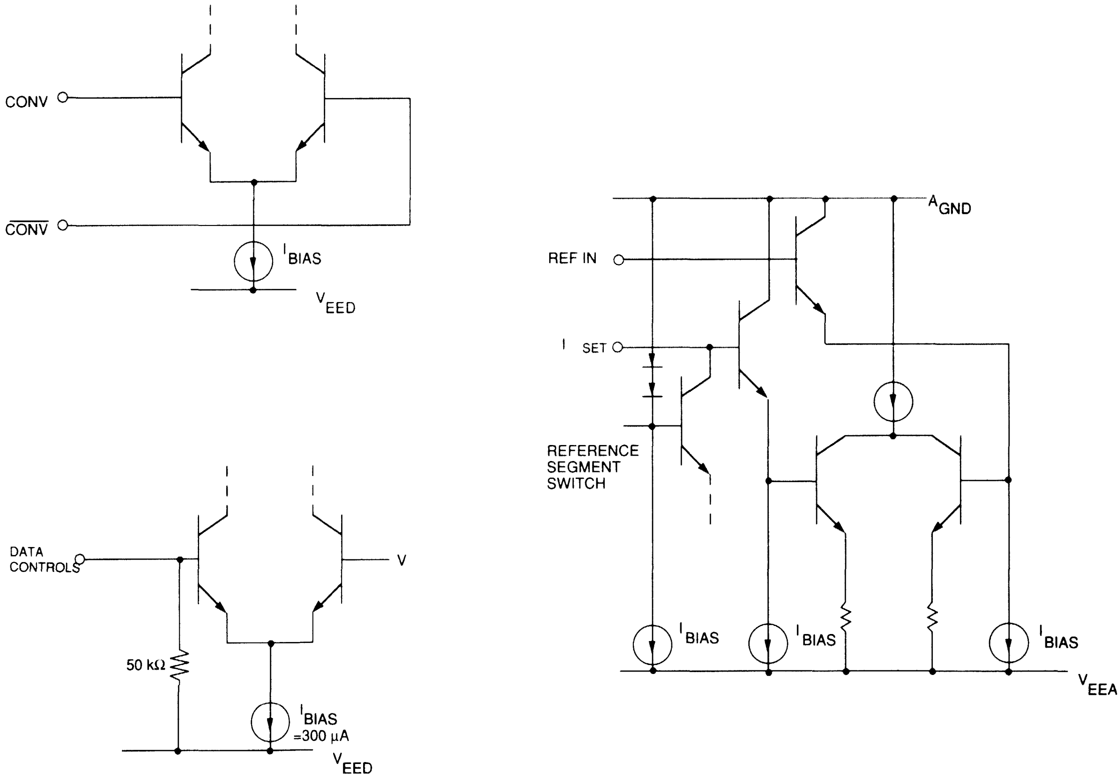
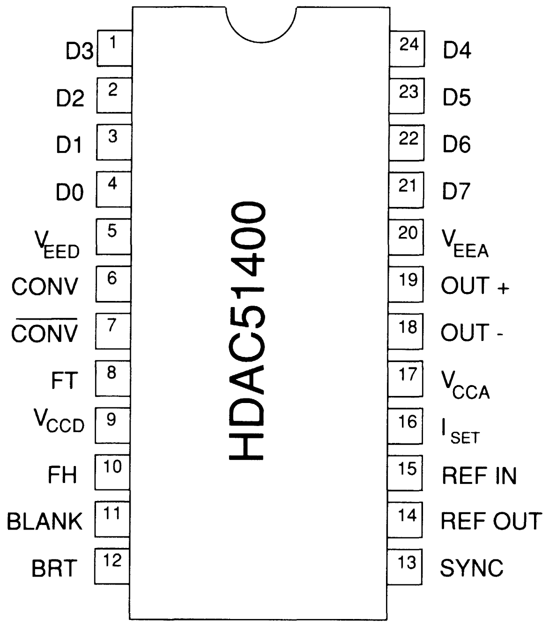


Figure 9 - Equivalent Input Circuits - Data, Clock, Controls and Reference



PIN ASSIGNMENTS



24 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
V_{EED}	Digital Negative Supply
CONV	Convert Clock Input
$\overline{CONV}$	Convert Clock Input Complement
FT	Register Feedthrough Control
V_{CCD}	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF OUT	Reference Output
REF IN	Reference Input
I_{SET}	Reference Current
V_{CCA}	Analog Positive Supply
OUT -	Output Current Negative
OUT +	Output Current Positive
V_{EEA}	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

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4

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

HDAC52160

HIGH SPEED 16-BIT DAC

FEATURES

- Fast Settling Time - 150 nsec
- Excellent Linearity T. C. -.3 ppm/°C
- On-Chip Band-Gap Voltage Reference
- On-Chip Application Resistors for Gain Selection
- TTL Compatible Inputs

APPLICATIONS

- High Speed Analog-to-Digital Converters
- Automatic Test Equipment
- Digital Attenuators
- Digital Communication Equipment
- Waveform Generators

4

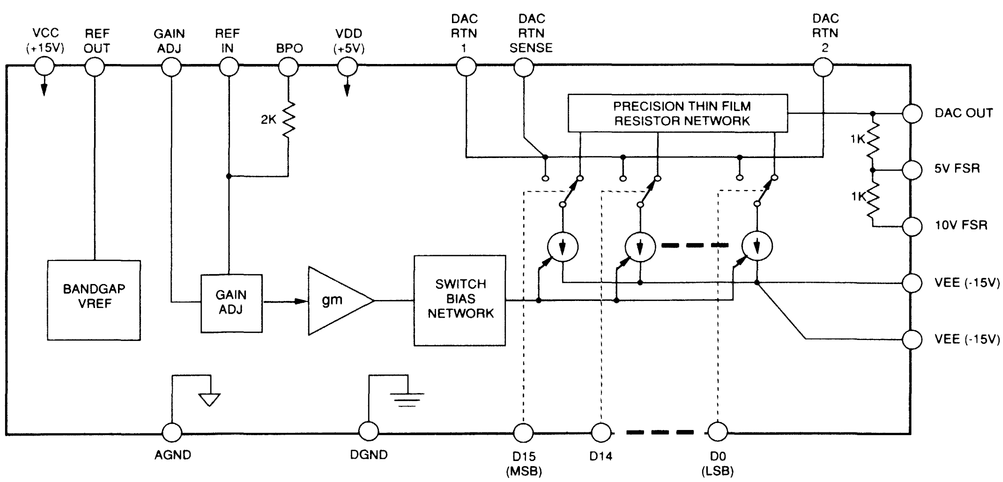
GENERAL DESCRIPTION

The HDAC52160 is a monolithic, high-performance, 16-bit digital-to-analog converter with unmatched speed and accuracy. With its 150 nanosecond settling time it is the highest speed 16-bit DAC in the industry. Unique features include the band-gap voltage reference and precision application resistors which greatly simplify device application. Unlike other high speed DACs, the HDAC52160 can be used in either a current-output or voltage-output mode.

The internal application resistors support output range selections of 0 to +10, 0 to +5, -5 to +5, and -2.5 to +2.5 volts. These internal resistors, used in conjunction with an external op amp, provide current-to-voltage conversion. Because of the high compliance voltage of the DAC output (+/- 2.5 volts), the HDAC52160 can also provide a direct voltage drive into a high impedance load without an external op amp.

The HDAC52160 operates with ±15 volt analog supplies, a separate +5 V digital supply and separate analog and digital grounds to provide maximum noise immunity. All logic input levels are TTL and 5 volt CMOS compatible. Laser-trimmed thin film technology ensures accuracy over time and environmental changes.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) 25 °C (1)

Supply Voltages

V_{CC} to AGND .... +18 V
V_{EE} to AGND .... -18 V
V_{DD} to DGND .... +6 V
AGND to DGND Differential .... +0.5 V

Input Voltages

All Digital Inputs to DGND .... -0.3 V to (V_{DD} +0.3 V)
REF IN to AGND .... 0 to +10 V

Temperature

Temperature, case .... -60 to +140 °C
junction .... +150 °C
Lead Temperature (soldering 10 seconds) .... +300 °C
Storage Temperature .... -65 to +100 °C

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
Note 2: Minimum air flow 50 LPM

RECOMMENDED OPERATING CONDITIONS

Supply Voltages

V_{CC} to AGND .... +14.25 to +15.75 V
V_{EE} to AGND .... -14.25 to -15.75 V
V_{DD} to DGND .... +4.75 to +5.25 V

Temperature

Temperature, Ambient (1) .... -25 to +85 °C

ELECTRICAL SPECIFICATIONS

T_A = -25 to +85 °C, V_{CC} = 15 V, V_{DD} = 5 V, V_{EE} = -15 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC52160A MIN	HDAC52160A TYP	HDAC52160A MAX	HDAC52160B MIN	HDAC52160B TYP	HDAC52160B MAX	HDAC52160C MIN	HDAC52160C TYP	HDAC52160C MAX	UNIT
ACCURACY SPECIFICATIONS												
Integral Linearity Error	TA=25 °C	I		±.0008	±.0015		±.0015	±.003		±.0045	±.006	%FSR
Integral Linearity Error		I		±.0015	±.003		±.0030	±.0045		±.005	±.012	%FSR
Integral Linearity Drift		IV		±0.3			±0.3			±0.3		PPM/°C
Differential Linearity Error	T_A=25 °C	I		±.0015	±.003		±.003	±.0045		±.0045	±.012	%FSR
Differential Linearity Error		I		±.0030	±.0045		±.0045	±.006		±.006	±.012	%FSR
Differential Linearity Drift		IV		±0.5			±0.5			±0.5		PPM/°C
Gain Error	T_A=25°C	I		±.03	±.15		±.03	±.15		±.03	±.15	%FSR
Gain Error		I		±.08	±.25		±.08	±.25		±.08	±.25	%FSR
Gain Error Drift		IV		±20			±20			±20		PPM/°C
Unipolar Offset Error	T_A=25°C	I		±.02	±.1		±.02	±.1		±.02	±.1	%FSR
Unipolar Offset Error		I		±.02	±.3		±.02	±.3		±.02	±.3	%FSR
Bipolar Offset Error	T_A=25°C	I		±2.5	±10		±2.5	±10		±2.5	±10	mV
Bipolar Offset Error		I		±5	±15		±5	±15		±5	±15	mV
DAC OUTPUT SPECIFICATIONS												
I_{OUT}		V		5			5			5		mA
R_{OUT}		V		1k			1k			1k		Ω
C_{OUT}	See Fig. 1	V		12			12			12		pF
Output Compliance[2]		V		±2.5			±2.5			±2.5		V
Output Noise	BW = 1 MHz	V		40			40			40		μV RMS

ELECTRICAL SPECIFICATIONS

T_A = -25 to +85 °C, V_{CC} = 15 V, V_{DD} = 5 V, V_{EE} = -15 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC52160A MIN	HDAC52160A TYP	HDAC52160A MAX	HDAC52160B MIN	HDAC52160B TYP	HDAC52160B MAX	HDAC52160C MIN	HDAC52160C TYP	HDAC52160C MAX	UNIT
DYNAMIC SPECIFICATIONS												
Settling Time	to .0015%	IV			150			150			150	ns
LOGIC SPECIFICATIONS												
V_{IH} [3]		I	3.75			3.75			3.75			V
V_{IL} [4]		I			1.5			1.5			1.5	V
I_{IH}		I		2	20		2	20		2	20	µA
I_{IL}		I		1	10		1	10		1	10	µA
REFERENCE												
Reference Output Voltage	T_A=25 °C	I	4.99	5	5.01	4.99	5	5.01	4.99	5	5.01	V
Reference Output Voltage		I	4.98	5	5.02	4.98	5	5.02	4.98	5	5.02	V
Max. Reference Output Load[5]	Total Current	IV		8			8			8		mA
Output Noise [6]	BW = 1 MHz	IV		40			40			40		µV RMS
POWER SUPPLIES												
V_{CC} Supply Current		I		4	6		4	6		4	6	mA
V_{EE} Supply Current		I		20	35		20	35		20	35	mA
V_{DD} Supply Current		I		6	9		6	9		6	9	mA
Power Dissipation		I		450	660		450	660		450	660	mW
PSRR, V_{CC}	+15 V±5%	V		.001			.001			.001		%G/%PS
PSRR, V_{EE}	-15 V±5%	V		.01			.01			.01		%G/%PS
PSRR, V_{DD}	+5 V±5%	V		.001			.001			.001		%G/%PS

Note 2: Accuracy is not guaranteed beyond this limit.
Note 3: Accuracy is not guaranteed below this limit.
Note 4: Accuracy is not guaranteed above this limit.
Note 5: Reference Load: REF IN = 1 mA BPO = 2.5 mA
Note 6: Reference decoupled as shown in Figure 6.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

TERMINOLOGY

INTEGRAL LINEARITY ERROR

Integral linearity error is a measure of the maximum deviation from a straight line passing through the end points of the DAC transfer function. It is measured after adjusting for zero offset error and zero gain error.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error is the difference between the measured change and the ideal 1 LSB change between two adjacent codes. A specified differential nonlinearity of <1 LSB ensures monotonicity and no missing codes.

OFFSET ERROR AND GAIN ERROR

Offset error is the absolute difference between actual and theoretical output voltage at code all 1s.

Gain error will be the difference between the measured and ideal full scale output range (after offset has been adjusted to zero) expressed as a percent of the ideal output level. The actual full scale output contains both the gain error and the offset error. Both offset and gain errors are adjustable to zero using the external trim network shown in Figures 4 and 5 respectively.

OUTPUT COMPLIANCE

Output compliance is the allowable range of voltage swing for pin DAC OUT. Other specifications, such as integral nonlinearity, are not guaranteed beyond the specified output compliance voltage.

GENERAL CIRCUIT DESCRIPTION

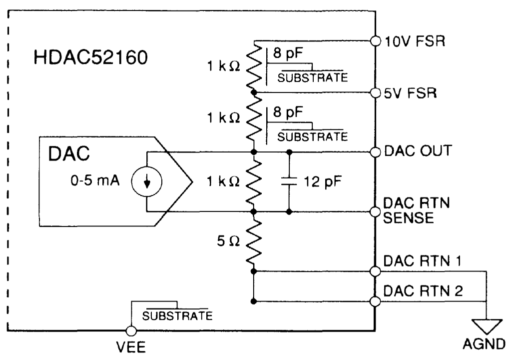
The HDAC52160 uses a unique design approach to set a new standard in monolithic DAC performance. It delivers exceptional 16-bit accuracy and stability over temperature and, at the same time, exhibits an extremely fast 150 ns settling time. On chip support functions include a stable band-gap voltage reference and application resistors for output scaling. Inclusion of these functions reduces the external analog component requirements and further increases accuracy. Digital circuitry on the chip is kept to a minimum (limited to the digital inputs), thus minimizing internal noise generation and providing interface flexibility.

DAC CIRCUITRY

The HDAC52160 uses current source segmentation for the most significant bits and an R-2R ladder for the least significant bits. The ladder, which consists of a resistor network, successively divides the (remaining) reference current to produce a binary weighted current division. In other words, in moving down the ladder, each 2R resistor leg has half the current flow of the previous leg. Each 2R resistor leg is connected to a current source that is trimmed during manufacturing to provide the 16-bit accuracy. Bipolar switches within each leg are controlled by the respective data bits (pins D0 through D15). When the controlling data bit is low, the 2R resistor leg current is steered to pin DAC OUT. When the data bit is high, the leg current is steered to the DAC RTN pins (DAC RTN 1, and DAC RTN 2), which are externally connected to analog ground.

Figure 1 illustrates the equivalent output circuit of the HDAC52160 showing on-chip application resistors and parasitic capacitances.

Figure 1 - Equivalent HDAC52160 Output Circuit



APPLICATION INFORMATION

ACTIVE CURRENT - TO - VOLTAGE CONVERSION

In many DAC applications the output current needs to be converted into a usable voltage signal. The most common current-to-voltage configuration for the HDAC52160 output is shown in Figure 2. Here, an external op amp in conjunction with the internal feedback resistor(s) is used for current-to-voltage (I-to-V) conversion. The op amp provides both a buffered Vout and maintains DAC OUT at a virtual ground. This way, Vout can provide up to a 10 volt output swing (using internal feedback resistors) and the Output Compliance specification (±2.5 volts maximum) is met.

Vout swing is determined by the feedback resistance. For a 5 volt Vout swing, the op amp's output is connected to pin 5 V FSR ("Full Scale Range") which provides an internal 1 kΩ feedback resistance. A 10 volt Vout swing is derived by connecting the op amp output to pin 10 V FSR. This feedback connection option is illustrated by the dotted line in Figure 2. Properly trimmed (as discussed later), the connections of Figure 2 as indicated, would result in the ideal output values as listed in Table I.

Figure 2 - Connection of External OP AMP for Active Current-to-Voltage Conversion

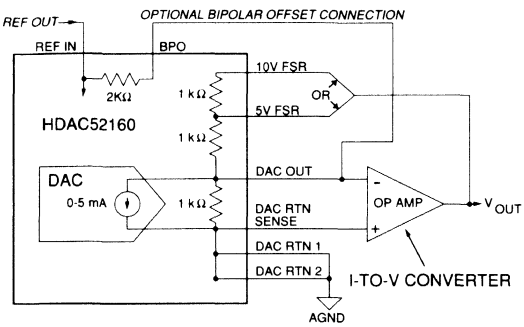


Table I - Normalized voltage values for programmable Output Ranges. (Using Figure 6)

INPUT CODE	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 VOLT	10 VOLT	5 VOLT	10 VOLT
1111 1111 1111 1111	0	0	- 2.50 V	- 5.00 V
1111 1111 1111 1110	+ 76.3 μV	+ 152.6 μV	- 2.499924 V	- 4.999846 V
0111 1111 1111 1111	+ 2.500 V	+ 5.00 V	0.00 V	0.00 V
0000 0000 0000 0000	+4.999924 V	+ 9.999846 V	+2.499924 V	+ 4.999846 V

To configure the bipolar output range as indicated in Table I, the BPO pin is connected to DAC OUT. This connection option is illustrated in Figure 2; this offsets the output range by half of the full scale range, so that a half-scale digital input value results in a output current value of zero.

The pin connections for the active I-to-V ranges supported by the internal application resistors are summarized in Table II.

OPERATIONAL AMPLIFIER SELECTION

Selection of the external op amp involves understanding the final system performance requirements in terms of both speed and accuracy. To maintain the 16-bit accuracy provided by DAC OUT at Vout shown in Figure 2, the op amp open loop gain (Avol) must be 96 dB minimum. Any gain lower than this will contribute an error in the I-to-V conversion circuit. To maintain the 150 ns settling time capability provided by DAC OUT at Vout, the op amp must have a minimum gain bandwidth of 50 MHz and settling time of less than 100 ns to 0.0015% of full scale.

Table II - Device Pin Connection Summary for Output Range Programming. (Active I-to-V Conversion Only)

DEVICE PINS	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 VOLT	10 VOLT	5 VOLT	10 VOLT
BPO	NOT CONNECTED	NOT CONNECTED	CONNECTED TO DAC OUT	CONNECTED TO DAC OUT
5V FSR	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED
10V FSR	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT

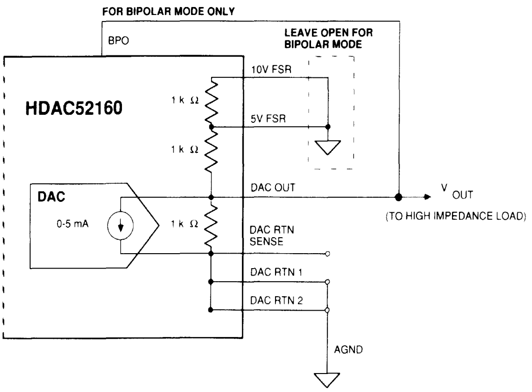
PASSIVE CURRENT-TO-VOLTAGE CONVERSION

Because of the HDAC52160's high voltage compliance, a voltage output can be derived directly at DAC OUT in a method suitable for some applications. By driving a load resistor directly with the current from DAC OUT, a voltage drop results producing Vout. An example of this implementation is shown in Figure 3, where an internal feedback resistor is used as the load 10 V FSR is grounded to optimize settling time). By utilizing all internal resistors, this circuit offers optimized stability and matching.

Output current from the DAC ranges between 0 and 5 mA, which corresponds to an input code of all 1s and all 0s, respectively. For unipolar mode, the net 500 Ω load of Figure 3 results in a -2.5 to 0 volt output range. For bipolar mode, the output voltage range is from +1.67 V to -1.67 V (typical). Both output ranges are within the specified output compliance limits. An external load resistor could also be used with this circuit, however there are difficulties with this arrangement; thermal tracking is not optimum, and the gain adjustment required to overcome the absolute internal resistance and DAC output current errors is beyond the correction range provided by the trim circuit, which is described later.

Note that the input resistance of the circuit driven by Vout will be placed in parallel with the load resistor. This hence limits the application of Figure 3 to high impedance loads. Also note that if a buffer (or other active circuit) is used at Vout in Figure 3, that circuit's CMRR must be at least 100 dB to maintain the DAC's accuracy. This is an advantage of the active current-to-voltage configuration shown in Figure 2, where the input of the op amp is always at virtual ground.

Figure 3 - Connection of Internal Load Resistors for Passive Unipolar/Bipolar Current-to-Voltage Conversion

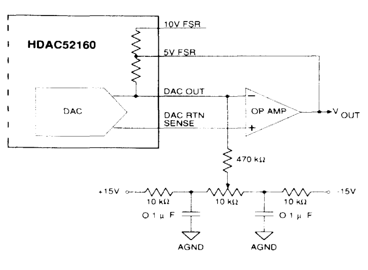


OUTPUT OFFSET COMPENSATION

Although the zero offset error of the HDAC52160 is within ±0.1% of the full scale range, some applications require better accuracy. The offset trim network of Figure 4, shown connected to DAC OUT, will allow offset adjustment in excess of ±0.2%. This trim network can be used for the active I-to-V conversion network of Figure 2 or the passive circuit of Figure 3. When using an external op amp as in Figure 2, optimum offset stability may be achieved by using the nulling network recommended by the op amp's manufacturer.

Although accuracy of the offset network components is not important, temperature tracking of the resistor and potentiometer values will affect offset trim stability. The resistors and potentiometer should have a low temperature coefficient and the potentiometer should be a high quality, multi-turn component to ensure minute adjustability and stability over time and temperature. The 0.1 µF capacitors shown (typically ceramic) are used to decouple power supply noise from the DAC output circuit.

Figure 4 - Offset Compensation



LOGIC INTERFACE

Because of the low logic input current specification, most TTL families will adequately drive the HDAC52160, even though minimum VIH is specified at 3.75 volts, a figure relatively high by TTL standards. Non-adherence to the VIH spec can result in a less than specified DAC accuracy. High-Speed CMOS logic (HC) or High-Speed CMOS logic with TTL compatible inputs (HCT) are directly compatible with the HDAC52160 logic inputs.

GAIN ADJUSTMENT

With the gain error of the HDAC52160 pre-trimmed to within ±0.15% of full scale accuracy, many applications require external gain adjustments. Configuration of the external gain adjustment network is shown is Figure 5. The adjustment potentiometer is connected between two low noise voltage sources, REF OUT and AGND, as shown. The two bypass capacitors shown further help to eliminate noise. Because of the voltage source asymmetry in relationship to the potentiometer wiper, the adjustment range is an asymmetric -0.6% to +1%. This adjustment range does sufficiently compensate for the error of the device, and the network will work for any type of output configuration. The adjustment range can be made larger and symmetrical by using a circuit similar to the offset compensation network as shown in Figure 4, but with the consequence of introducing power supply noise (and power supply variations) into the vital voltage reference circuit.

The selection criteria for the gain adjustment network components is similar to those described for the offset compensation network: accuracy is not as important as temperature stability.

Figure 5 - Gain Trim Network Suitable for All Output Configurations

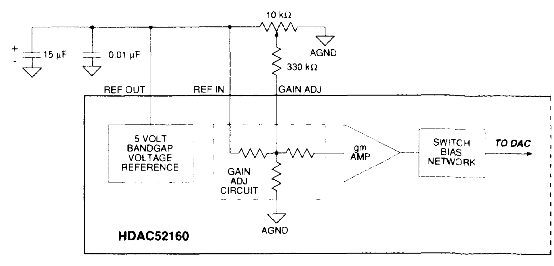
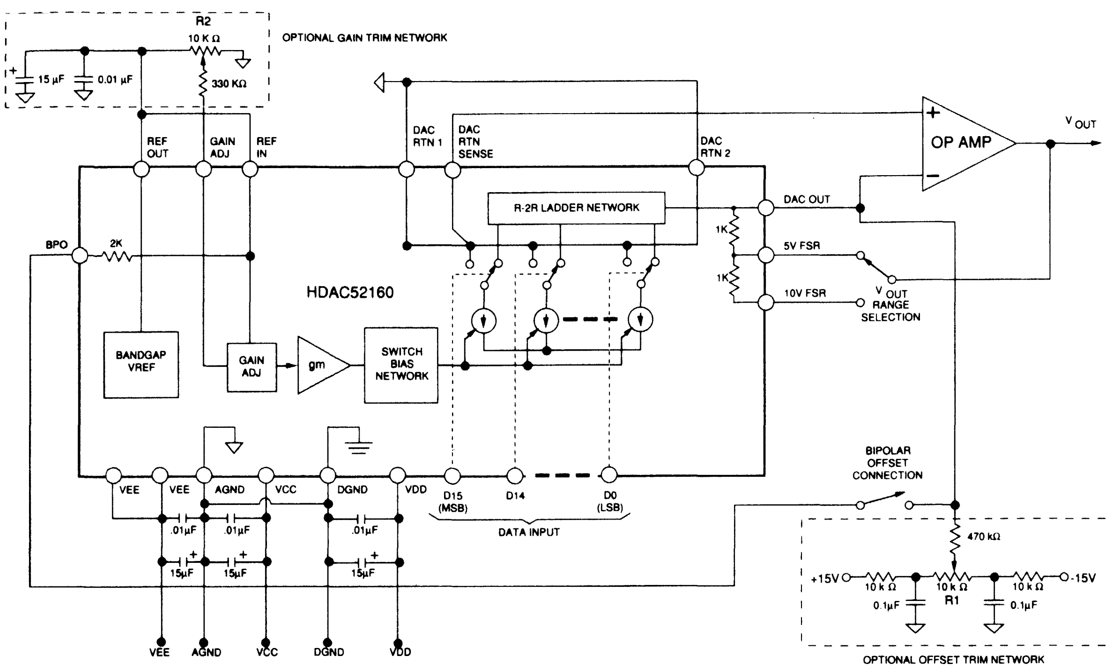


Figure 6 - Typical HDAC52160 Application Circuit



OFFSET AND GAIN CALIBRATION PROCEDURE

This calibration procedure is only applied to the I-to-V applications as shown in Figure 6.

The calibration consists of adjusting the "Vout" most negative voltage to its ideal value for the offset adjustment and adjusting the most positive "Vout" to its ideal value for gain adjustment. The offset and gain errors listed in the specifications for both Unipolar and Bipolar operation, may be adjusted to zero using R1 and R2 (see Figure 6) respectively. All components in the "optional offset trim network" and "optional gain trim network" shown in Figure 6 should have a low temperature coefficient. The potentiometers (R1 and R2) should be multi-turn components to insure minute adjustability.

If the adjustment is not needed, remove the "optional offset trim network" from the circuit.

Unipolar

The first step is offset adjustment. Set the input code to 1111 1111 1111 1111 and adjust R1 until Vout reads zero volts for either 5 V FSR operation or 10 V FSR operation.

Next is the gain adjustment. Set the input code to 0000 0000 0000 0000 and adjust R2 until Vout reads +4.999924 Volts for 5 V FSR operation or +9.999846 Volts for 10 V FSR operation.

Bipolar

For the Bipolar mode of operation, the calibration will start by adjusting the offset. Set the input code to 1111 1111 1111 1111 and adjust R1 until Vout reads -2.50000 Volts for 5 V FSR or -5.00000 Volts for 10 V FSR operation. The gain error calibration is done by setting the input code to 0000 0000 0000 0000 and adjusting R2 until Vout reads +2.499924 Volts for 5 V FSR operation or +4.999848 Volts for 10 V FSR operation.

CIRCUIT LAYOUT CONSIDERATIONS

In any analog system design, care must be taken in the circuit layout process. The design of a high-speed, 16-bit analog system offers an exceptional challenge. The integrity of the system's power supply and grounding is critical, and as with any precision analog component, good decoupling is needed directly at the device. Analog signal traces must be routed in a manner to minimize coupling from potential noise sources. With a 5 volt full-scale output voltage range, a mere 38 μVp-p noise level is equivalent to 1/2 LSB. Low amplitude noise such as this is virtually impossible to eliminate without totally shielding the analog circuit portion.

The power supply must be a well-regulated, noise-free analog voltage source. As with any analog device, the PSRR performance of the HDAC52160 degrades with higher frequency components. Logic noise in the supply or ground line contains high frequency components, so separate supplies and ground returns are recommended for the analog and logic portions of the system. Radiated noise from digital signal traces and power supply traces must also be avoided. Completely shield the analog circuit portion from digital circuitry and digital power supplies and ground. A separate analog ground plane near the device should be used to shield the digital data lines going into the device; this plane should have a trace that completely surrounds the digital inputs, if possible. If an analog ground plane is used with the device for shielding, keep the space between the digital ground plane and analog ground plane wide to prevent capacitive coupling. The best analog ground plane is one with the least resistance, i.e., the minimum total "squares" of surface area, regardless of size. All device grounding should be to the analog ground plane, except for the GND RTN pins which should be tied to the plane at one connection point only.

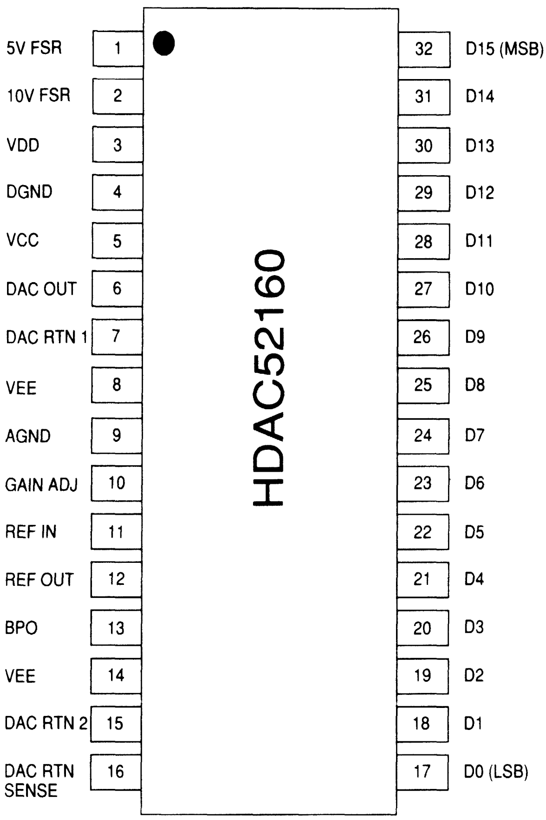
Figure 6 shows the implementation of decoupling devices (0.01 μF and 15 μF in parallel) at pin REF OUT. These devices should be connected to the analog ground and their incorporation will minimize the overall D/A conversion noise.

Since virtually all the interfacing to the HDAC52160 is analog in nature (the logic inputs are actually analog current switches), DGND and AGND should be tied together at the device and treated as an analog ground. This analog ground and the systems digital ground should be inter-tied only at a single point which has a low impedance path back to the system's power supplies. This will prevent modulation of the analog ground by digital power supply currents as well as digital noise injection.

The external components should be connected to the HDAC52160 with minimum length leads to help prevent noise coupling. The inputs of the external op amp are especially sensitive, so they should have short traces and be well shielded.

To the circuit driven by the HDAC52160, a voltage drop in the common analog ground will appear as a voltage offset. To avoid this, the HDAC52160 has provided a DAC SENSE pin which can be used for remote ground potential sensing.

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
5 V FSR	Output range scaling application resistor
10 V FSR	Output range scaling application resistor
VDD	+5 volt power supply connection
DGND	Digital ground connection
VCC	+15 volt power supply connection
DAC OUT	Analog current output of DAC
DAC RTN 1	DAC ground current return path
VEE	-15 volt power supply connection
AGND	Analog ground connection
Gain ADJ	Input reference trim adjustment
REF IN	Input for internal or external reference
REF OUT	Output of internal reference
BPO	Output offsetting application resistor
VEE	-15 volt power supply connection
DAC RTN 2	DAC ground current return path
DAC RTN SENSE	DAC ground current sense connection
D0	Input data bit 0 (LSB)
D1	Input data bit 1
D2	Input data bit 2
D3	Input data bit 3
D4	Input data bit 4
D5	Input data bit 5
D6	Input data bit 6
D7	Input data bit 7
D8	Input data bit 8
D9	Input data bit 9
D10	Input data bit 10
D11	Input data bit 11
D12	Input data bit 12
D13	Input data bit 13
D14	Input data bit 14
D15	Input data bit 15 (MSB)

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

HCMP96850

SINGLE ULTRA FAST VOLTAGE COMPARATOR

SPT
SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- Propagation Delay of 2.4 ns (Typ.)
- Propagation Delay Skew <300 ps
- Low Offset ±3 mV
- Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

GENERAL DESCRIPTION

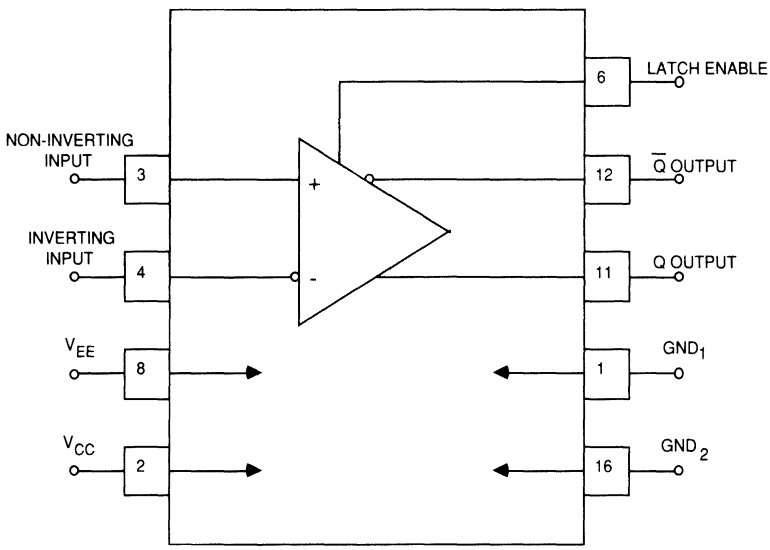
The HCMP96850 is a single, very high speed monolithic comparator. It is pin-compatible with and has improved performance over the AD9685 and the AM6685. The HCMP96850 is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96850 is available in a 16 lead DIP or in die form.

5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} Measured to GND) .... -0.5 to +6.0 V
Negative Supply Voltage (V_{EE} to GND)..... -6.0 to +0.5 V
Ground Voltage Differential.........................-0.5 to +0.5 V

Input Voltages

Input Voltage..-4.0 to +4.0 V
Differential Input Voltage.............................-5.0 to +5.0 V
Input Voltage, Latch Controls.........................V_{EE} to 0.5 V

Output

Output Current..30 mA

Temperature

Operating Temperature, ambient............ -25 to +85 °C
junction......................+150 °C
Lead Temperature, (soldering 60 seconds)........ +300 °C
Storage Temperature.............................. -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V ±.25 V, V_{EE} = -5.2 V ±.3 V, R_L = 50 Ohms, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	R_S = 0 Ohms	IV	-3		+3	mV
Input Offset Voltage (V_{os})	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$	IV	-3.5		+3.5	mV
(V_{os}) Tempco		V		4		µV/°C
Input Bias Current		I		4	±20	µA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		7		µA
Input Offset Current		I	-1.0		+1.0	µA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	IV	-1.5		+1.5	µA
Positive Supply Current		I		3.3	5	mA
Negative Supply Current		I		13.5	18	mA
Common Mode Range		I	-2.5		+2.5	V
Open Loop Gain		V		4000		V/V
Input Resistance		V		60		kΩ
Input Capacitance		V		3		pF
Input Capacitance	(LCC Package)	V		1		pF
Power Supply Sensitivity	V_{CC} and V_{EE}	V		70		dB
Common Mode Rejection Ratio		V		80		dB
Power Dissipation	I_{OUTPUT} = 0 mA	IV		90	120	mW

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V ±.25 V, V_{EE} = -5.2 V ±.3 V, R_L = 50 Ohms, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
OUTPUT LOGIC LEVELS (ECL 10 KH Compatible)						
Output High	50 Ohms to -2 V	I	-.98		-.81	V
Output Low	50 Ohms to -2 V	I	-1.95		-1.63	V
AC ELECTRICAL CHARACTERISTICS[1]						
Propagation Delay	10mV O.D.	III		2.4	3.0	ns
Latch Set-up Time		III		0.6	1	ns
Latch to Output Delay	50 mV O.D.	III			3	ns
Latch Pulse Width		V		2		ns
Latch Hold Time		III			0.5	ns
Rise Time	20% to 80%	V		1.76		ns
Fall Time	20% to 80%	V		1.76		ns

Note 1: 100 mV input step

TEST LEVEL CODES

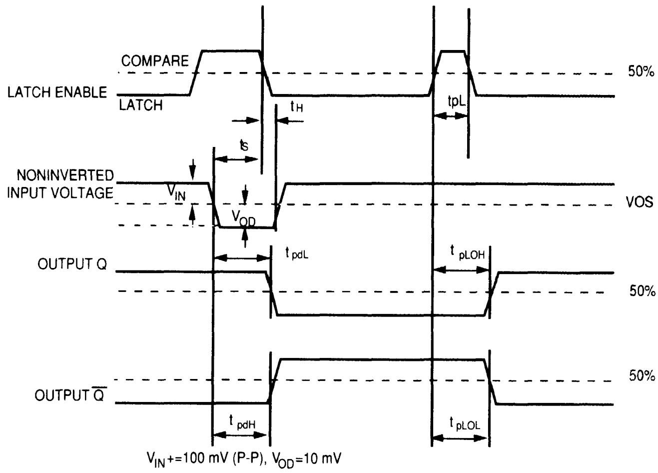
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Figure 1 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may or may not be detected.

SWITCHING TERMS (refer to Figure 1)

t_{pdH} — INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crossed the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pdL} — INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

t_{pLOH} — LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} — LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

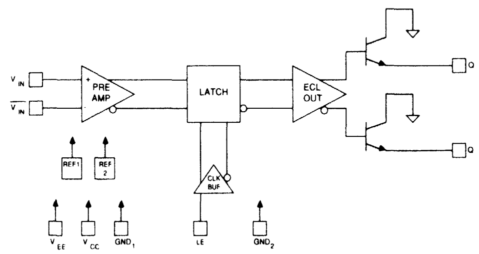
t_H — MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} — MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S — MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

V_{OD} — VOLTAGE OVERDRIVE.

INTERNAL FUNCTION DIAGRAM



GENERAL INFORMATION

The HCMP96850 is an ultra high speed single voltage comparator. It offers tight absolute characteristics which guarantee matching from package to package. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 Ohm transmission lines.

The HCMP96850 has one latch enable control and can be driven by standard ECL logic. It also has two separate ground pins, one for the output to accommodate large ground currents without affecting the rest of the circuit, while the other is for the small signal intermediate stages. The input stage is referenced to V_{CC} and V_{EE}.

This comparator offers the following improvements over existing devices:

- Short propagation delays
- Low offset voltage and temperature coefficient
- Low power
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

TYPICAL INTERFACE CIRCUIT

A typical interface circuit using the comparator is shown in Figure 2. Although it needs few external components and is easy to apply, there are several considerations that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96850 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately one-half inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end of the characteristic impedance of the line to prevent reflections. The HCMP96850 is capable of driving 50 Ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated N/C should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

The timing diagram for the comparator is shown in Figure 1. The latch enable (LE) pulse is shown at the top. If LE is high in the HCMP96850, the comparator tracks the input difference voltage. When LE is driven low, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of 10 mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the latch enable falling edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 Ohms to ground while unused latch enable pins should be connected directly to ground.

Figure 2 - Typical Interface Circuit

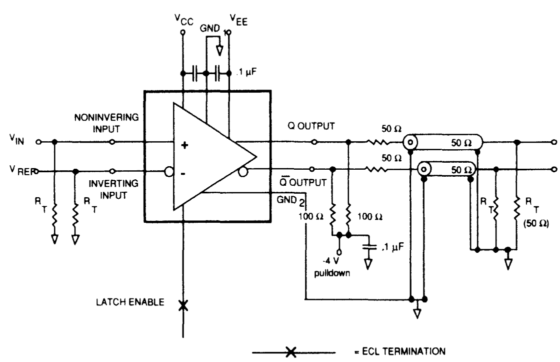


Figure 3 - Equivalent Input Circuit

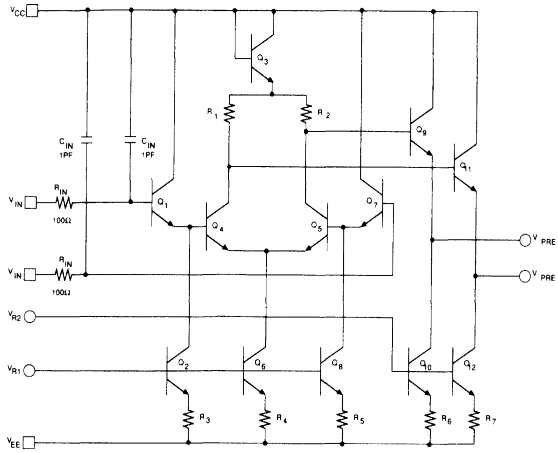


Figure 4 - Output Circuit

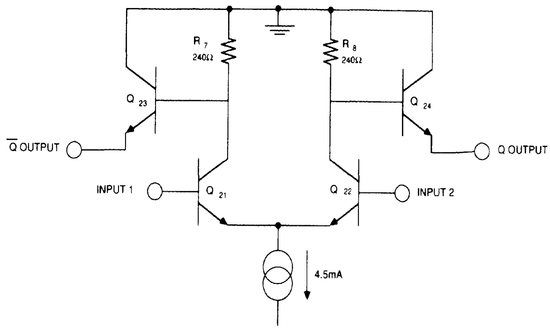


Figure 5A - Test Load

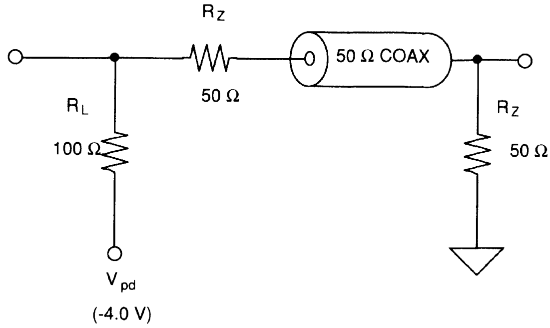
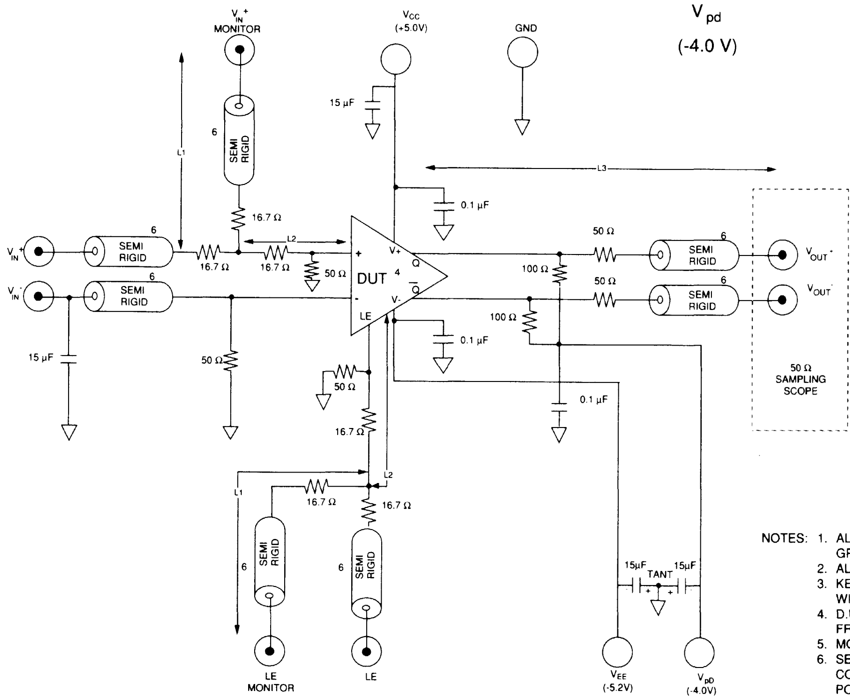
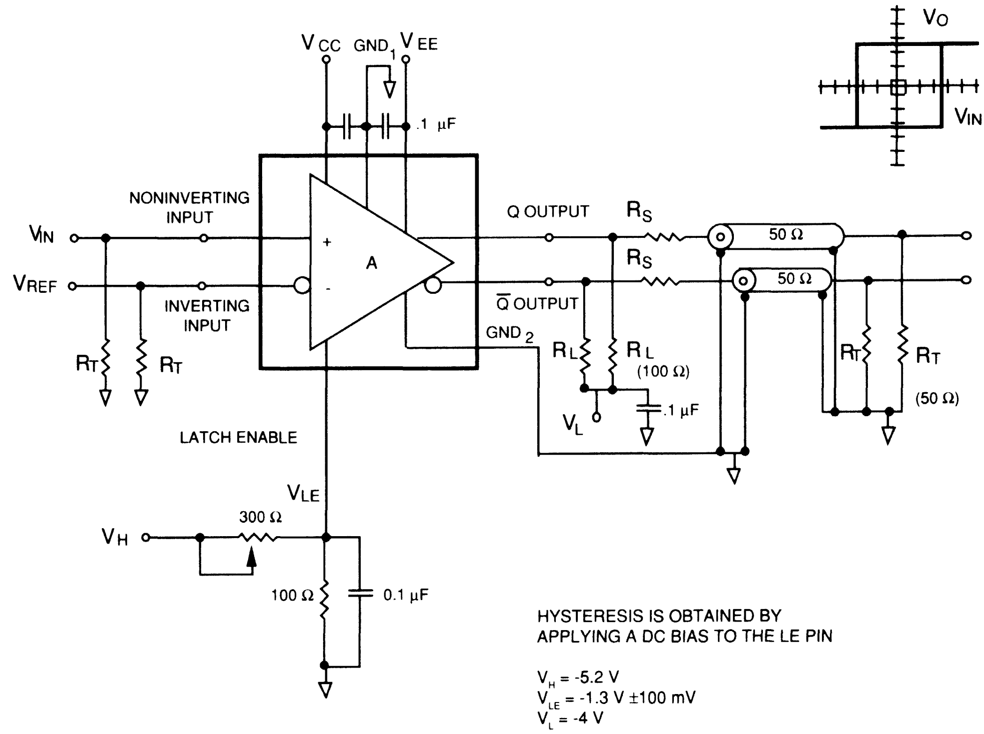


Figure 5B - AC Test Fixture



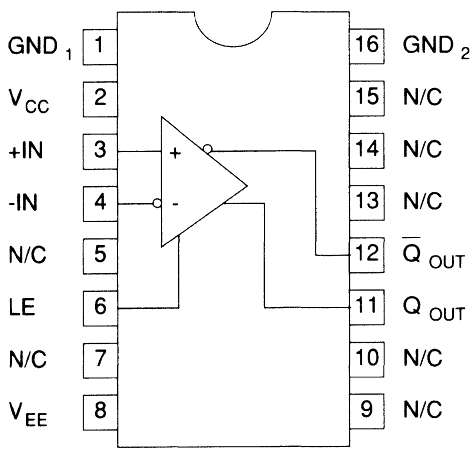
NOTES:
1. ALL BNC & SEMIRIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (10 Ω = 49.9 Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
4. D.U.T. PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50 Ω TO GND.
6. SEMIRIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

Figure 6 - HCMP96850 with Hysteresis



PIN ASSIGNMENTS

TOP VIEW



16 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
GND_1	Circuit Ground
V_{CC}	Positive Supply Voltage
+IN	Noninverting Input
-IN	Inverting Input
N/C	No Connection
LE	Latch Enable
V_{EE}	Negative Supply Voltage
Q_{OUT}	Output
$\overline{Q}_{OUT}$	Inverted Output
GND_2	Output Ground

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

HCMP96870A

DUAL ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay <2.3 ns
- Propagation Delay Skew <300 ps
- 300 MHz Minimum Tracking Bandwidth
- Low Offset ±3 mV
- Low Feedthrough and Crosstalk
- Differential Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

GENERAL DESCRIPTION

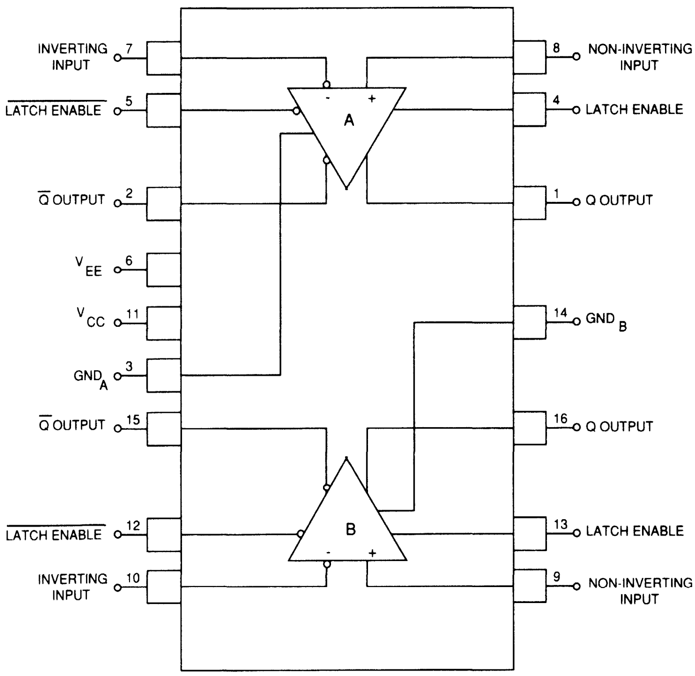
The HCMP96870A is a dual, very high speed monolithic comparator. It is pin-compatible with, and has improved performance over AMD's AM6687 and Analog Devices AD9687. The HCMP96870A is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96870A is available in a 16 lead cerdip, 16 lead PDIP, 20 contact leadless chip carrier (LCC), 20 lead PLCC, and in die form.

5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} Measured to GND) .... -0.5 to +6.0 V
Negative Supply Voltage (V_{EE} to GND)..... -6.0 to +6.0 V
Ground Voltage Differential..........................-0.5 to +0.5 V

Input Voltages

Input Voltage...-4.0 to +4.0 V
Differential Input Voltage..............................-5.0 to +5.0 V
Input Voltage, Latch Controls.........................V_{EE} to 0.5 V

Output

Output Current...30 mA

Temperature

Operating Temperature, ambient.................0 to +70 °C
junction......................+150 °C
Lead Temperature, (soldering 60 seconds)........ +300 °C
Storage Temperature.............................. -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE (-25 to +85 °C)

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.20 V, R_L = 50 Ohm, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	R_S = 0 Ohms	III	-3	±.5	+3	mV
Input Offset Voltage	R_S = 0 Ohms, $T_{MIN}<T_A<T_{MAX}$	IV	-3.5		+3.5	mV
Offset Voltage Tempco		V		4		µV/°C
Input Bias Current		I		6	±20	µA
Input Bias Current	$T_{MIN}<T_A<T_{MAX}$	IV		7	±38	µA
Input Offset Current		I	-1.0		+1.0	µA
Input Offset Current	$T_{MIN}<T_A<T_{MAX}$	IV	-1.5		+1.5	µA
Positive Supply Current		I		7	10	mA
Negative Supply Current		I		27	36	mA
Common Mode Range		I	-2.5		+2.5	V
Open Loop Gain		V		4000		V/V
Input Resistance		V		60		kΩ
Input Capacitance		V		3		pF
Input Capacitance	(LCC Package)	V		1		pF
Power Supply Sensitivity	V_{CC} and V_{EE}	IV	50	100		dB
Common Mode Rejection Ratio		IV	50	85		dB

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE (-25 to +85 °C)

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.20 V, R_L = 50 Ohm, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Power Dissipation	I_{OUTPUT} = 0 mA	I		185	250	mW
OUTPUT LOGIC LEVELS (ECL 10 KH Compatible)						
Output High	50 Ohms to -2 V	I	-.98		-.81	V
Output Low	50 Ohms to -2 V	I	-1.95		-1.63	V
AC ELECTRICAL CHARACTERISTICS[1]						
Propagation Delay	10 mV OD	III		2.0	2.3	ns
Latch Set-up Time		III		0.6	1	ns
Latch to Output Delay	50 mV OD	III			3	ns
Latch Pulse Width		V		2		ns
Latch Hold Time		III			0.5	ns
Rise Time	20% to 80%	V		1.2		ns
Fall Time	20% to 80%	V		1.2		ns
Min Clock Rate		V		300		MHz

Note 1. 100 mV input step.

TEST LEVEL CODES

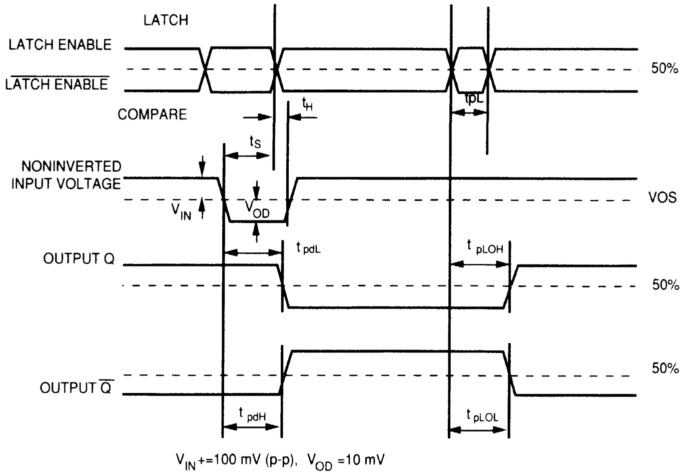
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Figure 1 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_s and t_H may not be detected (LE is the inverse of $\overline{LE}$).

SWITCHING TERMS (refer to Figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crossed the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

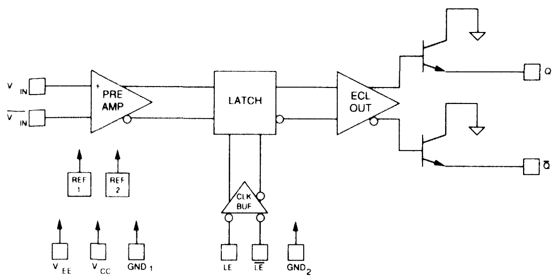
t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

$t_{pdL} - t_{pdH}$ DIFFERENTIAL PROPAGATION DELAY (SKEW) INPUT TO OUTPUT - The delay or skew between comparators.

INTERNAL FUNCTIONAL DIAGRAM



GENERAL INFORMATION

The HCMP96870A is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The HCMP96870A has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

The dual comparator shares the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

This comparator offers the following improvements over existing devices:

- Shorter propagation delays
- Lower offset voltage and temperature coefficient
- Lower overall system power
- Better rejection between comparator channels
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in Figure 2. Although it needs few external components and is easy to apply, there are several conditions that should be met to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96870A comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, and the input impedance to the part should be kept as low as possible to decrease parasitic feedback. If the output board traces are longer than approximately one-half inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The HCMP96870A is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

The timing diagram for the comparator is shown in Figure 1. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low in the HCMP96870A, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states. Please note that the Latch Enable and $\overline{\text{Latch Enable}}$ notations are not consistent with the industry standard; these names have always been opposite to the pins' functional descriptions. Please see the timing diagram in Figure 1 for absolute clarification.

The leading edge of the input signal (which consists of 10 mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the latch enable falling edge and LE rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 ohms to ground while unused latch enable pins should be connected to the appropriate supplies: ground or V_{EE}.

Figure 2 - Typical Interface Circuit

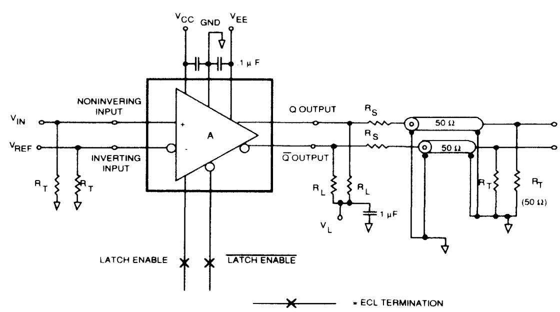


Figure 3 - Equivalent Input Circuit

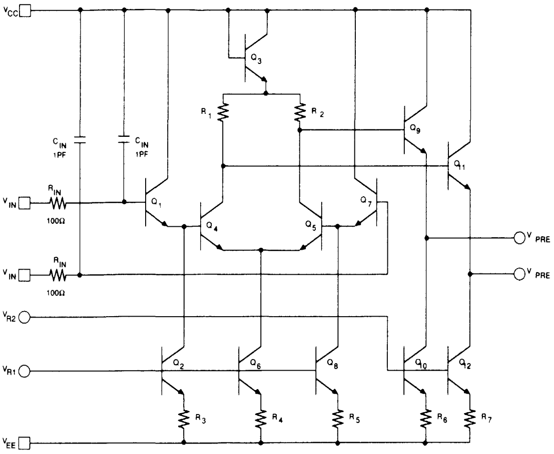


Figure 4 - Output Circuit

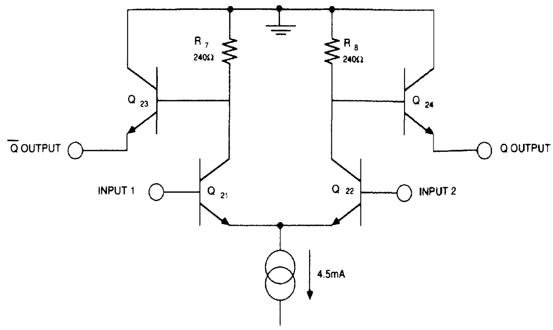


Figure 5A - Test Load

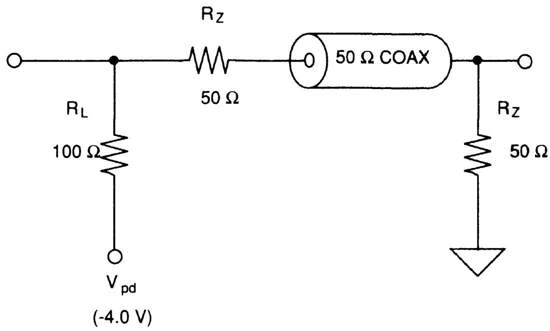
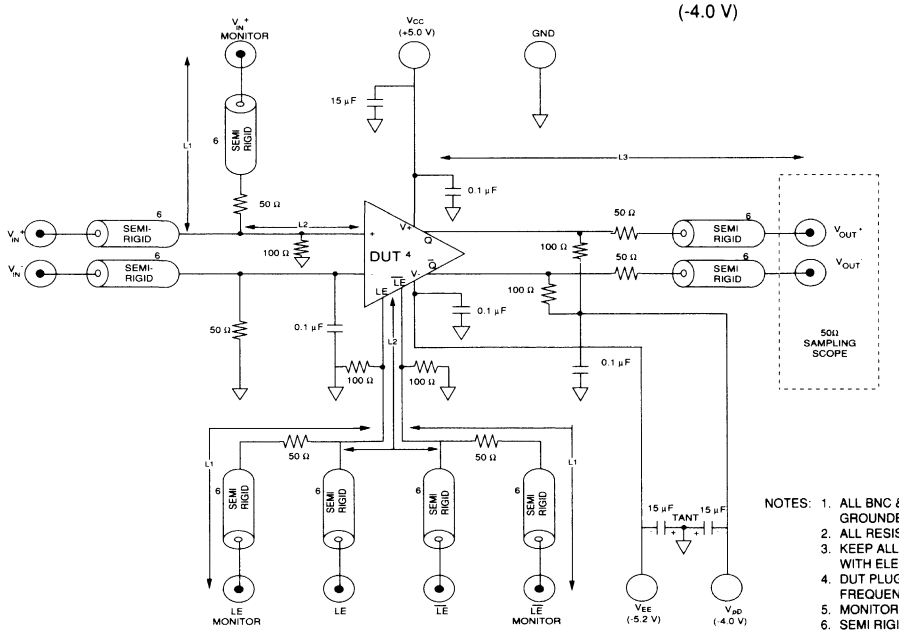
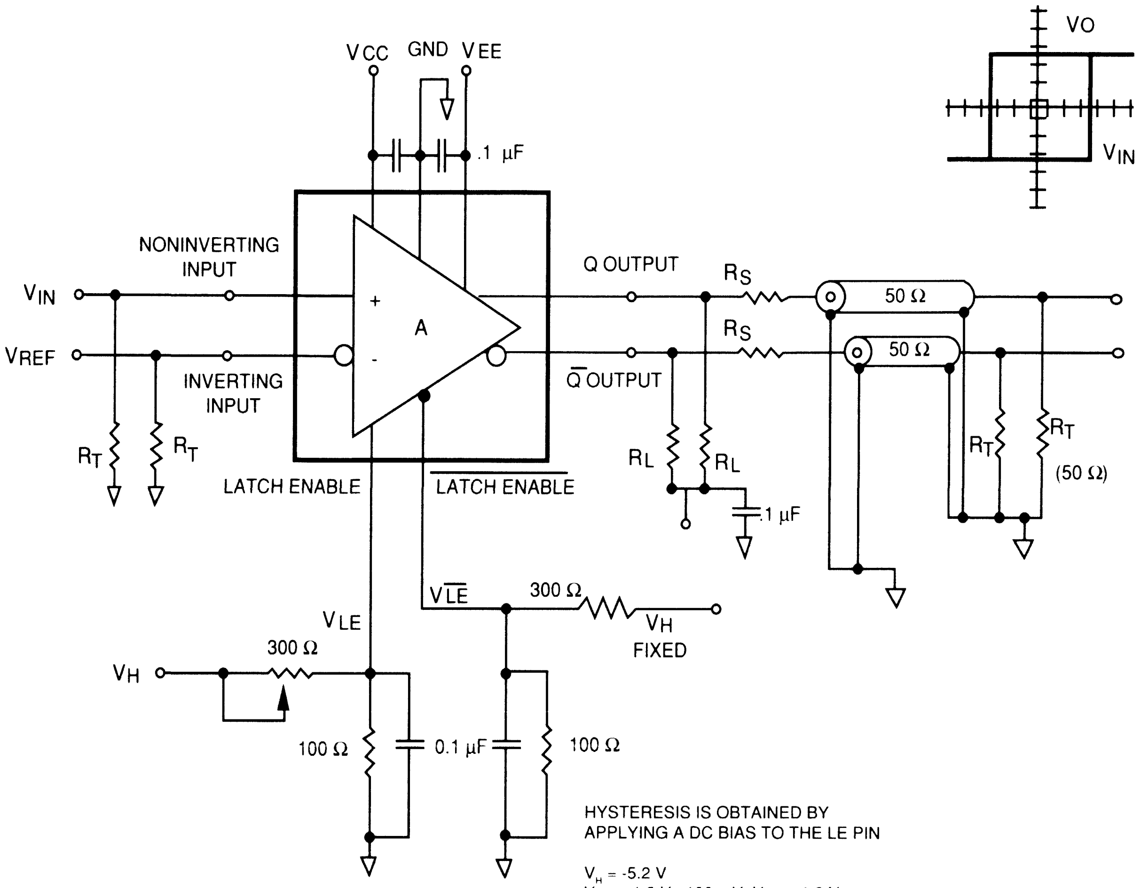


Figure 5B - AC Test Fixture



NOTES:
1. ALL BNC & SEMI RIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (50 Ω = 49.9 Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
4. DUT PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50 Ω TO GND.
6. SEMI RIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

Figure 6 - HCMP96870A with Hysteresis

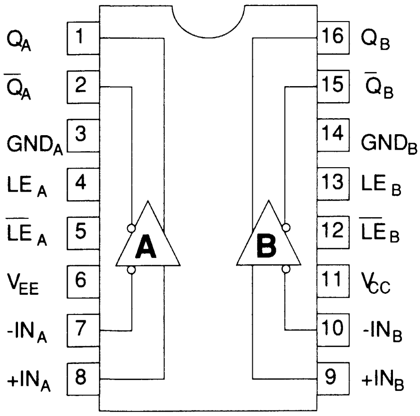


HYSTERESIS IS OBTAINED BY
APPLYING A DC BIAS TO THE LE PIN

V_H = -5.2 V
V_{LE} = -1.3 V ±100 mV, $V_{\overline{LE}}$ = -1.3 V
V_L = -4.0 V

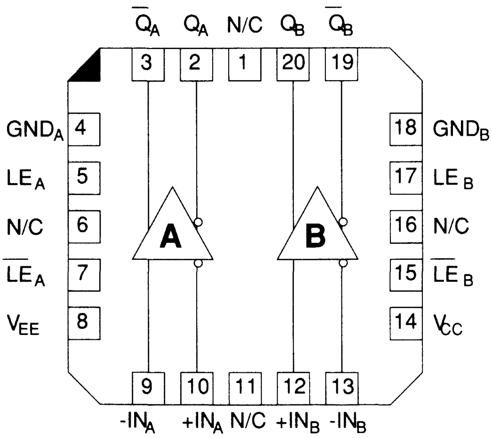
PIN ASSIGNMENTS

TOP VIEW



16 LEAD DIP

TOP VIEW



20 CONTACT CERAMIC LCC/PLCC

PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
LE_A	Inverted Latch Enable A
$\overline{LE}_A$	Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Inverted Latch Enabled B
$\overline{LE}_B$	Latch Enable B
GND_B	Ground B
Q_B	Inverted Output B
$\overline{Q}_B$	Output B

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5

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

SPT9689

DUAL ULTRA-FAST VOLTAGE COMPARATOR

PRELIMINARY INFORMATION

FEATURES

- 650 ps Propagation Delay
- 100 ps Propagation Delay Variation
- 900 MHz Tracking Bandwidth
- 70 dB CMRR
- Low Feedthrough and Crosstalk
- Differential Latch Control
- ECL Compatible

APPLICATIONS

- Automated Test Equipment
- High Speed Instrumentation
- Window Comparators
- High Speed Timing
- Line Receivers
- High Speed Triggers
- Threshold Detection
- Peak Detection

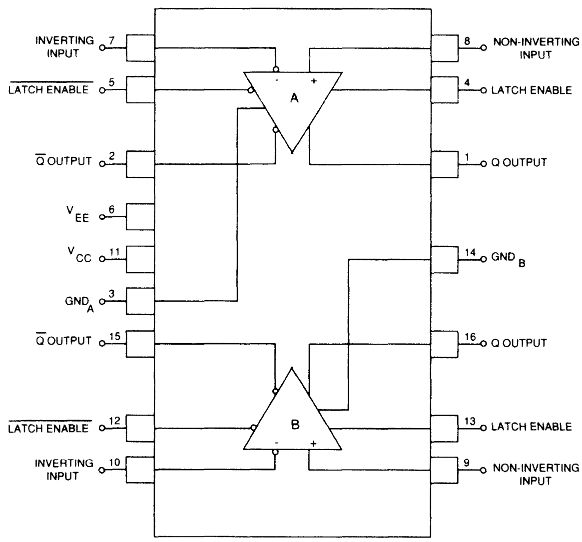
GENERAL DESCRIPTION

5

The SPT9689 is a *Sub*-nanosecond monolithic dual comparator. The propagation delay variation is less than 100 ps from 5 mV to 50 mV input overdrive voltage. The input slew rate is 10 V/ns. The device utilizes a high precision differential input stage with a common-mode range of -2.5 V to +4.0 V.

ECL compatible complimentary digital outputs are capable of driving 50 Ω terminated transmission lines and providing 30 mA output drive. The SPT9689 is pin-compatible to HCMP96870 and is available in 20 lead LCC, 16 lead ceramic sidebrazed DIP and die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages

Positive Supply Voltage (V_{CC} Measured to GND) .... -0.5 to +6.0 V
Negative Supply Voltage (V_{EE} to GND) .... -6.0 to +0.5 V
Ground Voltage Differential .... -0.5 to +0.5 V

Input Voltages

Input Common Mode Voltage .... -4.0 to +5.0 V
Differential Input Voltage .... -3.0 to +3.0 V
Input Voltage, Latch Controls .... V_{EE} to 0.5 V

Output

Output Current 30mA

Temperature

Operating Temperature, ambient .... -55 to +125°C
junction .... +150°C
Lead Temperature, (soldering 60 seconds) .... +300°C
Storage Temperature .... -65 to +150°C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE (-25 to +85 °C)

T_A = +25 °C V_{CC} = +5.0 V ±.25 V, V_{EE} =-5.20 V,RL = 50 Ohm to -2 V, unless otherwise specified.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9689A MIN	TYP	MAX	SPT9689B MIN	TYP	MAX	UNITS
Input Offset Voltage	$V_{IN,CM}$=0	I		3.0	10		12	25	mV
Input Offset Voltage	$V_{IN,CM}$=0 $T_{MIN}<T_A<T_{MAX}$	III		4.5	15		15	30	mV
Offset Voltage Tempco		V		10			40		µV/°C
Input Bias Current		I		±8	±20		±8	±20	µA
Input Bias Current	$T_{MIN}<T_A<T_{MAX}$	IV		±12	±30		±12	±30	µA
Input Offset Current		I		±1.0	±3.0		±2.0	±5.0	µA
Input Offset Current	$T_{MIN}<T_A<T_{MAX}$	IV		±2.0	±5.0		±4.0	±7.0	µA
Positive Supply Current	Dual	I		18	30		18	35	mA
Negative Supply Current	Dual	I		40	55		40	60	mA
Common Mode Range		I	-2.5		+4.0	-2.5		+4.0	V
Open Loop Gain		V		66			66		dB
Differential Input Resistance		V		500			500		kΩ
Input Capacitance	Cerdip Package	V		2.0			2.0		pF
Input Capacitance	LCC Package	V		0.6			0.6		pF
Power Supply Sensitivity		V		70			70		dB

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE (-25 to +85 °C)

T_A = +25 °C, V_{CC} = +5.0 V ±.25 V, V_{EE} = -5.20 V, R_L = 50 Ohm to -2 V, unless otherwise specified.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9689A MIN	SPT9689A TYP	SPT9689A MAX	SPT9689B MIN	SPT9689B TYP	SPT9689B MAX	UNITS
Common Mode Rejection Ratio	Vcmv=-2.0 to +4.0	V		70			70		dB
Power Dissipation	Dual, Without Load	I		350	425		350	475	mW
Power Dissipation	Dual, With Load	I		400	550		400	550	mW
Output High Level	ECL 50 Ohms to -2V	I	-1.00		-.81	-1.00		-.81	V
Output Low Level	ECL 50 Ohms to -2V	I	-1.95		-1.54	-1.95		-1.54	V

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Propagation Delay	20 mV O.D.	III		650	850		750	950	ps
Latch Set-up Time		V		450	600		450	600	ps
Latch to Output Delay	50 mV O.D.	V		350	500		350	500	ps
Latch Pulse Width		V		500			500		ps
Latch Hold Time		V		30			30		ps
Rise Time	20% to 80%	V		180			180		ps
Fall Time	20% to 80%	V		80			80		ps
Slew Rate		V		10			10		V/ns
Bandwidth	-3 dB	V		900			900		MHz

CAUTION: ESD SENSITIVE DEVICE

ELECTRICAL CHARACTERISTICS TESTING

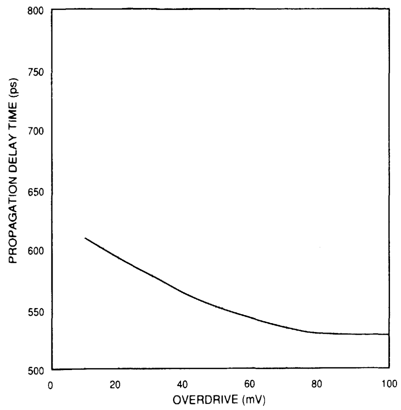
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

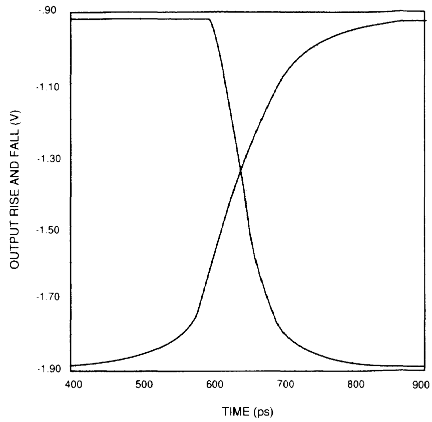
Unless otherwise noted, all tests are pulsed tests, therefore $T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

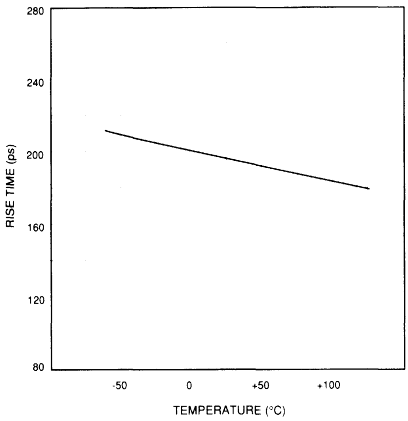
PROPAGATION DELAY VS OVERDRIVE VOLTAGE



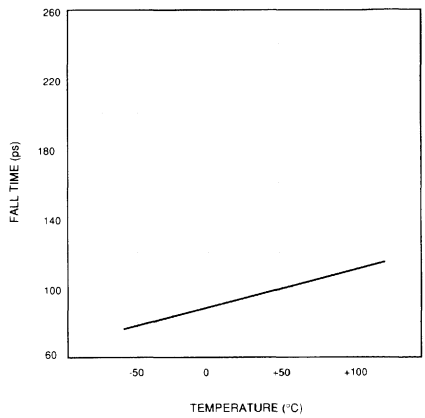
RISE AND FALL OF OUTPUTS VS TIME CROSSOVER



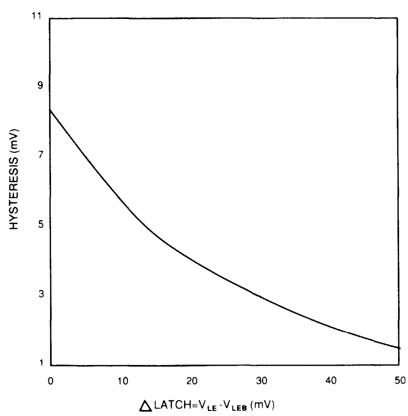
RISE TIME VS TEMPERATURE



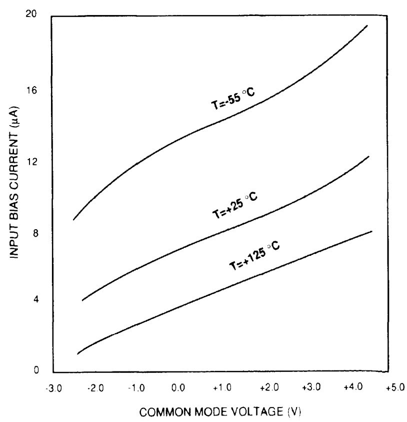
FALL TIME VS TEMPERATURE



HYSTERESIS VS △ LATCH



INPUT BIAS CURRENT VS COMMON MODE VOLTAGE



GENERAL INFORMATION

The SPT9689 is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9689 has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

The negative common mode voltage is -2.5 V. The positive common mode voltage is +4.0 V.

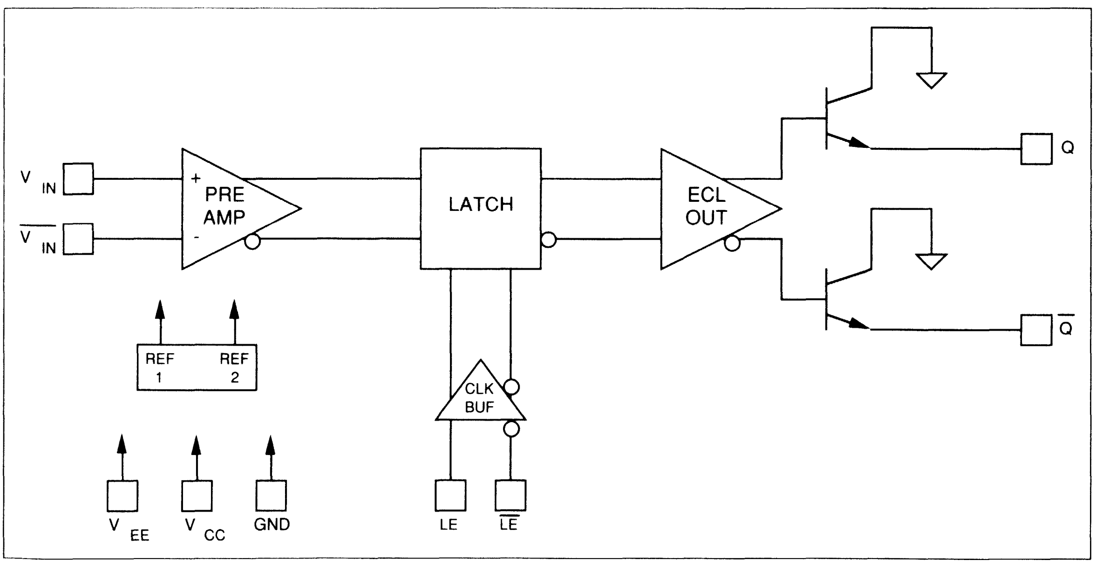
The dual comparators share the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

This comparator offers the following improvements over existing devices:

- Proprietary design techniques such as precision clamping of the gain stages result in well behaved and stable output transient response
- Ultra-fast propagation delay time of 650 ps
- Very low propagation delay skew of less than 100 ps in response to input overdrive of +5 to +50 mV
- Excellent input and output rejection between comparator channels
- Hysteresis can be programmed by using LE and $\overline{LE}$ pins to stabilize the output
- Low offset voltage, temperature coefficient and thermal tails

All of these combined features produce high performance products with timing stability and repeatability for large system precision.

INTERNAL FUNCTION DIAGRAM



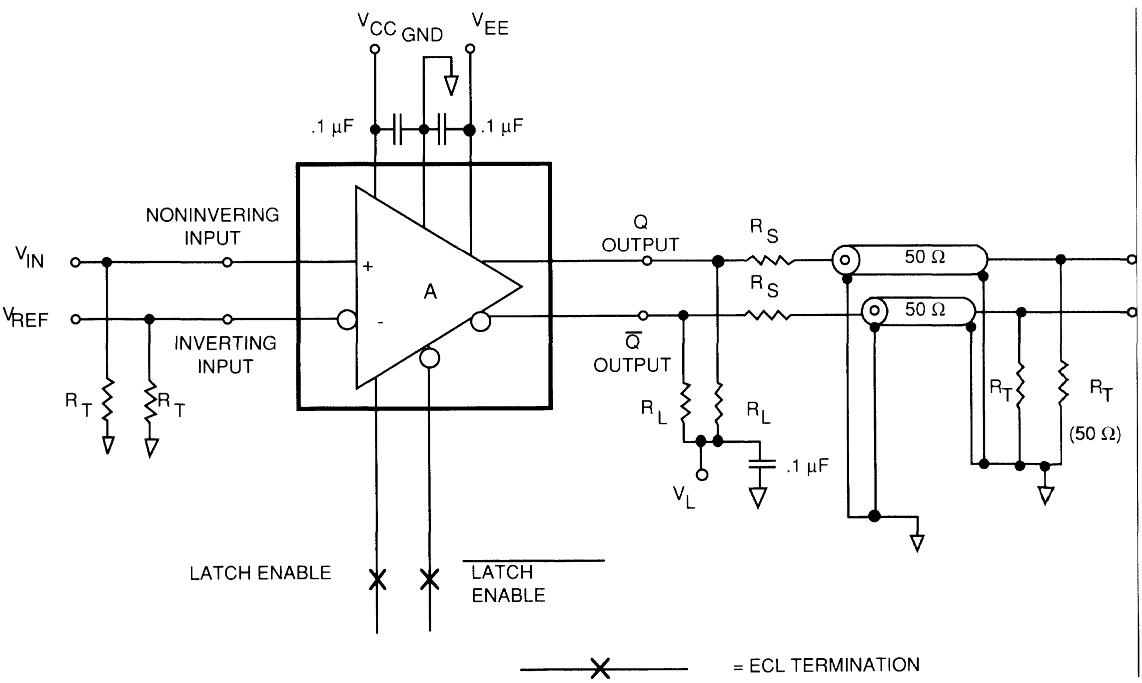
TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in Figure 1. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the SPT9689 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The SPT9689 is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

FIGURE 1 SPT9689 TYPICAL INTERFACE CIRCUIT



TIMING INFORMATION

The timing diagram for the comparator is shown in Figure 1. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low in the SPT9689, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

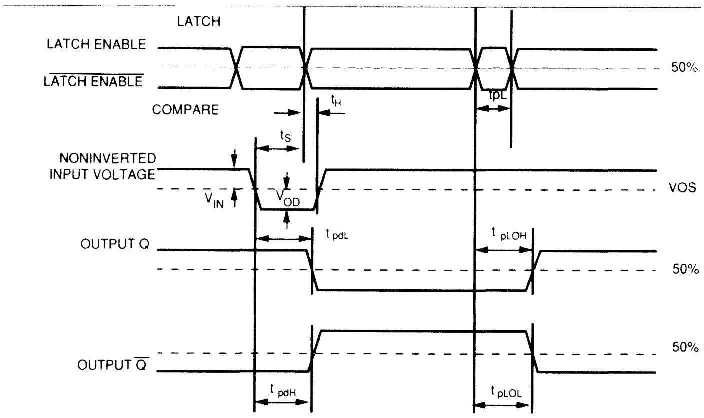
The leading edge of the input signal (which consists of 10mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the latch enable falling edge and LE rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be termined with 50 ohms to ground while unused latch enable pins should be connected directly to ground.

SPT9689

5

Figure 2 - Timing Diagram



V_{IN} = 100 mV (p-p), V_{OD} = 10 mV

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_s and t_H may not be detected.

SWITCHING TERMS (refer to Figure 2)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal voltage to the 50% point of an output LOW to HIGH transition

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal reaches the input overdrive voltage to the 50% point of an output HIGH to LOW transition

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to 50% point of an output LOW to HIGH transition

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition

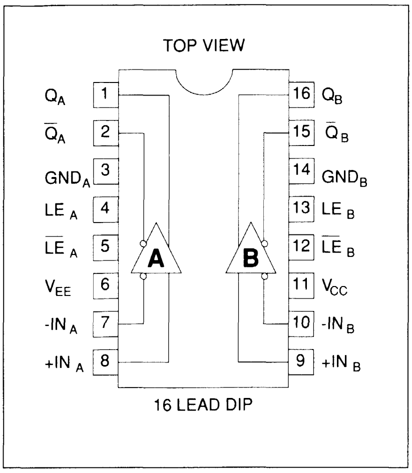
t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs

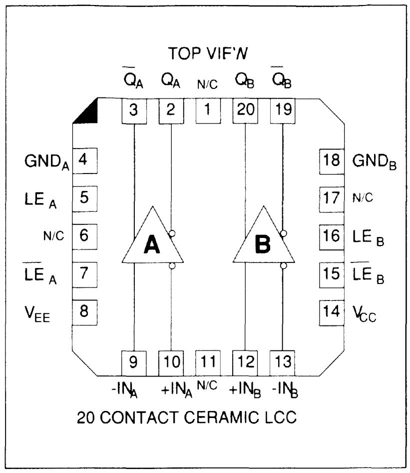
t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs

V_{OD} VOLTAGE OVERDRIVE

PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
LE_A	Inverted Latch Enable A
$\overline{LE}_A$	Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Inverted Latch Enabled B
$\overline{LE}_B$	Latch Enable B
GND_B	Ground B
Q_B	Inverted Output B
$\overline{Q}_B$	Output B

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5

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

HSCF24040

PROGRAMMABLE 7TH ORDER LOW PASS ACTIVE FILTER

FEATURES

- 85 dB Dynamic Range
- Cut Off Frequency (*ƒ*c) up to 20 KHz
- On-Chip Anti-Aliasing Protection
- Programmable Bandedge Frequency for both RC and Switched Capacitor Filter
- S/H Output
- Microprocessor Compatible
- 7th Order Ladder Filter with cosine Prefiltering Stage
- Stopband Attenuation >76 dB at 3 *ƒ*c
- Programmable DC Gains of 1, 2, 4, 8
- On-Chip Oscillator (External Crystal)

APPLICATIONS

- High Performance Modems
- 12-Bit Signal Processing Systems
- Pre-Sample Anti-Alias Filter
- Test Equipment/Instrumentation
- Spectrum Analyzer
- Medical Telemetry/Filtering
- Speech Analysis and Synthesis
- Data Acquisition Systems
- Computer Controlled Test Systems

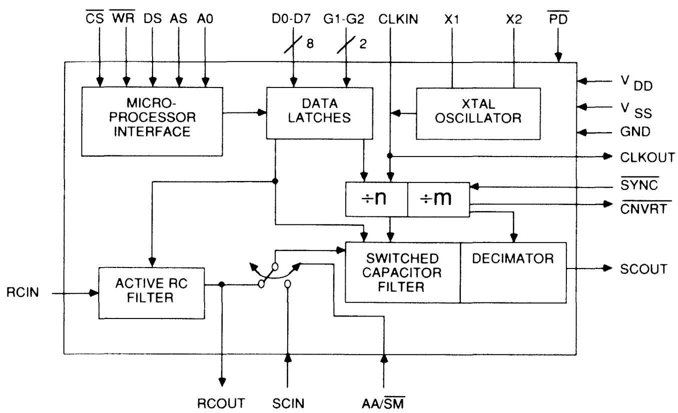
GENERAL DESCRIPTION

The HSCF24040 is a monolithic 7th order low pass active filter system. It offers 76 dB of stop-band attenuation and 85 dB of dynamic range wich makes it the first switched-capacitor filter suitable for 12-bit systems. Because of the internal 3rd order RC anti-aliasing filter, no external components are required for device operation. Both the RC filter and switched-capacitor filter have digitally programmable cut off frequencies.

The last stage of the SC filter contains a programmable decimator which provides a sample/hold output function that reduces the sample rate at SCOUT. This ensures that the hold period of the sample and held output is long enough to perform an A/D conversion or be resampled by an external S/H.

The HSCF24040 is manufactured using a BEMOS process which allows the fabrication of low power CMOS logic, linear CMOS circuits, bipolar linear circuitry and thin film resistors on a single chip. The HSCF24040 is packaged on a 32 pin DIP, operates on a ±5V supply voltage and is offered in commercial temperature range. Additionally, the HSCF24040 is available in a surface mount, 28 contact LCC with minimal microprocessor interface support.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond Which Damage May Occur) (1)

Supply Voltages
VDD to GND ....0 to +7V
VSS to GND ....0 to -7V

Input Voltages
Digital Input Voltages
All except CLKIN, $\overline{CS}$ ....-0.3V to (VDD +0.3V)
CLK, $\overline{CS}$ ....(VS -0.3V) to (VDD +0.3V)
Analog Input Voltages
SCIN< RCIN ....(VSS -0.3V) to (VDD +0.3V)

Output Voltages
Analog Output Voltages
SCOUT, RCOUT ....Momentary Short to VDD

Temperature
Temperature, case ....-60 to 140°C
junction ....+150°C
Lead Temperature (soldering 10 seconds) ....+300°C
Storage Temperature ....-65 to 150°C

Note (1): Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

VDD = +5V, VSS = -5V, T_A = 0 to 70°C, unless otherwise specified. All typical specifications are for T_A = 25°C only.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Gain of Combined RCF and SCF:						
HSCF24040ACJ						
SCF Gain Setting = 1.0	SCBW = 5 kHz	I	0.995	1.0	1.005	V/V
SCF Gain Setting = 2.0	RCBW = 7 kHz	I	1.99	2.0	2.01	V/V
SCF Gain Setting = 4.0		I	3.97	4.0	4.03	V/V
SCF Gain Setting = 8.0		I	7.92	8.0	8.08	V/V
DC Gain of RCF Only		I	0.95		1.05	V/V
DC Gain of SCF Only	SCF Gain Setting = 1.0	I	0.95		1.05	V/V
RCOUT Offset Voltage		I	-10		+10	mV
System Pedestal		III		80		mV
Output Drive Capability, RCOUT and SCOUT						
Maximum Voltage Swing	RL = 5 kΩ	I	+3.0			V
Minimum Voltage Swing	RL = 5 kΩ	I			-3.0	V
Maximum Sink/Source Current	RL = 5 kΩ	I	600			µA
Analog Input Voltage Range (1)						
RCIN		I	-3.0		+3.0	V
SCIN; SCF Gain Setting = 1.0		I	-3.0		+3.0	V
SCIN: SCF Gain Setting = 2.0		I	-1.5		+1.5	V
SCIN; SCF Gain Setting = 4.0		I	-0.75		+0.75	V
SCIN; SCF Gain Setting = 8.0		I	-0.375		+0.375	V
Analog Input Impedance						
RCIN Resistance		I	100			kΩ
RCIN Capacitance		II			25	pF
SCIN Resistance		I	50			kΩ
SCIN Capacitance		II			25	pF

ELECTRICAL SPECIFICATIONS

VDD = +5V, VSS = -5V, T_A = 0 to 70°C, unless otherwise specified. All typical specifications are for T_A = 25°C only.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Current						
IDD; Normal Mode	XTAL Oscillator Active	I		15	20	mA
IDD; Power Down Mode	XTAL Oscillator Active	I		2	4	mA
ISS; Normal Mode	XTAL Oscillator Active	I		15	18	mA
ISS; Power Down Mode	XTAL Oscillator Active	I		1	3	mA
Power Dissipation						
Normal Mode	XTAL Oscillator Active	I		150		mW
Power Down Mode	XTAL Oscillator Active	I		15		mW

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
RC FILTER (RL = 5 kΩ, CL = 50 pF)						
Programmable Bandwidth (Fo, -3dB)		I	7		80	kHz
Bandedge Tolerance, Referenced to Fo		I	-5		+5	%
Passband Response, DC to 0.25Fo Referenced to RCF DC Gain		I	-0.1		+0.1	dB
Stopband Loss, Referenced to RCF DC Gain						
0.25Fo		I			0.2	dB
Fo		I	2	3	4	dB
17.25Fo		I	72			dB
Harmonic Distortion, ±3V Sinusoidal Input at RCIN						
Magnitude of Harmonics		II		-80		dB
THD		I		0.01	0.02	%
Dynamic Range		II	85	90		dB
Integrated Noise Voltage, 0.01Fo to 2.0Fo		II		50	70	μV rms
SC FILTER (RL = 5 kΩ, CL = 50 pF)						
Programmable Bandwidth (Fc=-.1 dB)		I	78		20,000	Hz
Bandedge Tolerance, Referenced to Fc		I	-0.5		+0.5	%
Passband Response, DC to Fc Referenced to SCF DC Gain		I	-0.1		+0.1	dB
SC FILTER (RL = 5kΩ, CL = 50 pF)						
Stopband Loss, Referenced to SCF DC Gain						
1.5Fc		I	30			dB
2.0Fc		I	50			dB
2.5Fc		I	66			dB
3.0Fc		I	76			dB
Harmonic Distortion, ±3V Sinusoidal Input at SCIN						
Magnitude of Harmonics		II		-72		dB
THD		I		0.05	0.075	%

ELECTRICAL SPECIFICATIONS

VDD = +5V, VSS = -5V, T_A = 0 to 70°C, unless otherwise specified. All typical specifications are for T_A = 25°C only.

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
SC FILTER (RL = 5kΩ, CL = 50 pF)						
Dynamic Range		II	85	90		dB
Integrated Noise, Voltage, 0.01Fc to 2.0Fc		II		70	100	µV rms
DIGITAL INPUTS (Pins D0-D7, G1, G2, $\overline{SYNC}$, CLKIN, $\overline{PD}$, AA/$\overline{SM}$, A0, AS, DS, $\overline{CS}$, $\overline{WR}$)						
VIH (Input Voltage High)		I	2.0			V
VIL (Input Voltage Low)		I			0.8	V
IIN (Input Current)		I			1.0	µA
CIN (Input Capacitance)		II			10	pF
DIGITAL OUTPUTS (Pins CLKOUT, $\overline{CNVRT}$)						
VOL (Output Voltage Low)	Driving Standard TTL Load	I			0.4	V
VOH (Output Voltage High)	Driving Standard TTL Load	I	2.4			V
CLOCK FREQUENCY						
Internal Oscillator Frequency	External Xtal	I	1		4	MHz
Input Clock Frequency (Note: 2)		I			4	MHz
MICROPROCESSOR INTERFACE TIMING						
Non-Multiplexed Address/Data bus:						
Tas (Address Setup Time)		I	100			nsec
Tah (Address Hold Time)		I	10			nsec
MICROPROCESSOR INTERFACE TIMING						
Multiplexed Address/Data Bus:						
Tasm (Address Setup Time)		I	20			nsec
Tahm (Address Hold Time)		I	10			nsec
Tds (Data Setup Time)		I	100			nsec
Tdh (Data Hold Time)		I	10			nsec
Tdpw (Data Latch Pulse width, DS or $\overline{WR}$)		I	100			nsec
Taps (Address Latch Pulse Width)		I	50			nsec
Tcsh (Chip Select Hold, $\overline{CS}$ or $\overline{WR}$)		I	10			nsec
SCOUT SYNCHRONIZATION TIMING						
T1 (CLKIN to CLKOUT Delay)		I			50	nsec
T2 ($\overline{SYNC}$ Delay Time)		I	100			nsec
T3 ($\overline{SYNC}$ Setup Time)		I	75			nsec
T4 ($\overline{SYNC}$ Pulse Width) (Note: 3)		I	75			nsec
T5 (CLKIN to $\overline{CNVRT}$ Delay)		I			85	nsec

Notes:
1. Input voltages outside of these ranges will degrade harmonic distortion performance.
2. The minimum input clock frequency is constrained only by the SC filter bandwidth. SC bandwidths below 78 Hz may degrade at high temperatures due to leakage currents.
3. It is required that the external $\overline{SYNC}$ input return to a logic high at least 1 CLKIN clock cycle prior to the falling edge of the next $\overline{CNVRT}$ output.

TEST LEVEL CODES

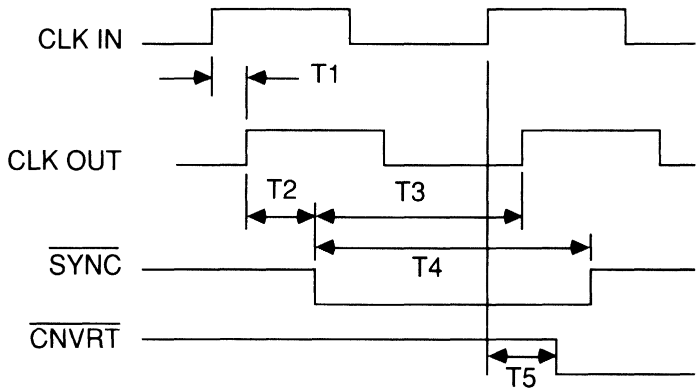
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

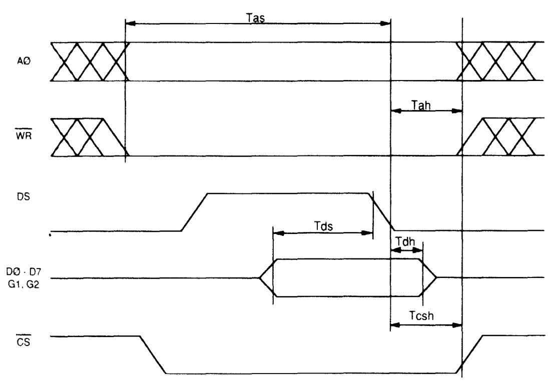
Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

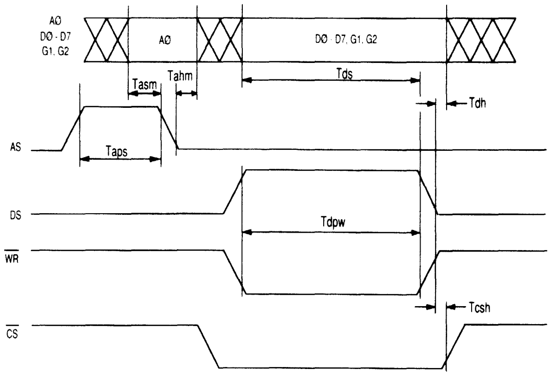
SCOUT SYNCHRONIZATION TIMING



TIMING DIAGRAM FOR NON-MULTIPLEXED BUS



TIMING DIAGRAM FOR MULTIPLEXED BUS



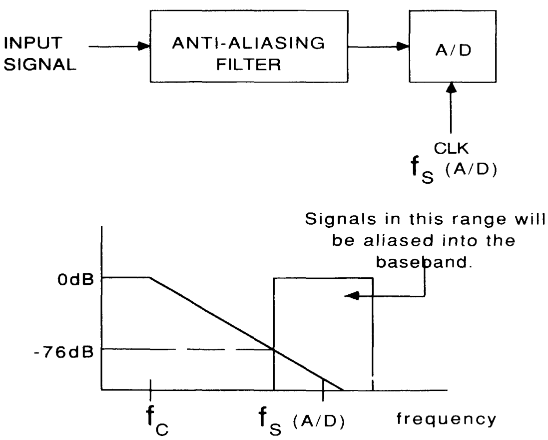
GENERAL DESCRIPTION

(Please refer to AN109 EB105 Evaluation Board and AN111 Analog/Digital Interface Requirements for addional information on the HSCF24040.)

SC FILTER

SC filters are sampled data filters that provide extremely accurate and stable responses. This is because their internal "time constants" depend only upon the switching frequency and the ratios of monolithic capacitors. The switching frequency is normally derived from a crystal controlled oscillator and is thus, extremely precise. On-chip capacitor ratios are accurate to within approximately 0.1%. Therefore, high order sharp rolloff filters can be manufactured that require no post production trimming. Since the filter bandedge can be programmed by varying the frequency of the clock that controls the filters switches, the filter bandedge can be made to track the sample rate of an external A/D converter. The filter in the HSCF24040 has 7 poles (Chebyshev approximation) to insure a minimum loss of 76 dB at 3 times the bandedge so that the system A/D can sample as low as 4 times the bandedge (see Figure 1). The SC filter has a differential signal path to improve its PSRR, distortion, and dynamic range. Through digital programming, bandedges of up to 20 KHz and DC gains of 1, 2, 4, or 8 can be achieved.

Figure 1 - Requirements for an Anti-Aliasing Filter Prior to A/D Conversion



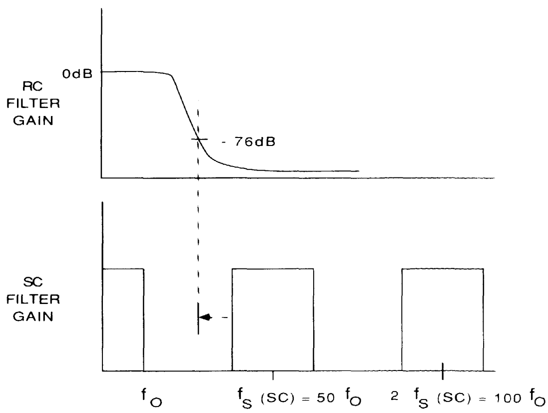
NOTE: Since the filter loss is greater than 76 dB, any aliased signals will be below the 12 bit level.

ACTIVE RC FILTER

Although the SC filter is programmable and offers excellent performance, it does have one major drawback. Because it is a sample data filter, it can fold or alias out-of-band energy into the desired passband in which the same way as the external A/D. Therefore a continuous-time filter is required in front of the SC filter to provide aliasing protection. We are, however, aided by the fact that the filter sampling rate is many times greater than the bandedge frequency (50 times in this case). Thus, a low order, active RC filter with a bandedge accuracy of only 5% will suffice. This concept is illustrated in Figure 2. The bandedge for this RC filter must be programmable to insure sufficient rejection of the SC filter images located at multiples of the SC filter rate. Eight different RC filter bandedges spanning a 12-to-1 range are available on the HSCF24040. The programmability is achieved by switching different resistor and capacitor values into the filter. A single RC filter bandwith setting (3 dB) of f_O (RCF) will provide 76 dB of anti-aliasing protection for SC filter bandwidths ranging from f_O (RCF)/5.71 to f_O (RCF)/4.

The topology of the RC filter has been chosen so that the DC gain and the pole Q's rely on ratio matching of the on-chip resistors and capacitors. The RC filter bandedge is laser trimmed for high accuracy during the manufacturing process.

Figure 2 - RC Filter Provides Anti-Aliasing for SC Filter



NOTE: The RC filter should provide >76 dB of loss for several different SC filter sample rates f_s (SC).

DECIMATOR

The decimator block samples the differential output of the SC filter and converts it to a single ended signal. The decimator also provides a sample-and-hold output (SCOUT) at a programmable sample rate of 25fc, 12.5fc, 6.25fc, or 4.167fc, where fc is the SC filter bandwidth. By choosing the proper decimation rate, the hold time at SCOUT will be sufficiently long to allow an A/D conversion to take place. (An external sample and hold may be required for hold times longer than 100 µsec to prevent more than 1/2 LSB of droop for a 12-bit A/D converter).

The $\overline{\text{CNVRT}}$ output is an active low digital output that indicates when the SCOUT output is valid. Applying a falling edge to the $\overline{\text{SYNC}}$ input initiates the $\overline{\text{CNVRT}}$ pulse on the next rising edge of CLKOUT. The use of the decimator block with $\overline{\text{SYNC}}$ and $\overline{\text{CNVRT}}$ insures the proper timing interface between SCOUT and an external A/D converter or sample and hold and eliminates the need for a smoothing filter at the SCOUT output.

PROGRAMMABILITY

The chip contains an 8-bit and a 2-bit data register. Data in the 8-bit register controls the SC filter bandedge, RC filter bandedge, and the decimation rate. (A programmable divide down chain generates the SC filter clocks from the master clock. A similar divide down chain determines the decimation rate from the SC filter clocks). Data in the 2-bit register controls the programmable D.C. gain of the SC filter. The truth tables for both registers are shown in Table I.

Table I - Programmable Features

RCF BANDEDGE

RCF 3dB BW	D7	D6	D5
80KHz	0	0	0
56KHz	0	0	1
40KHz	0	1	0
28KHz	0	1	1
20KHz	1	0	0
14KHz	1	0	1
10KHz	1	1	0
7KHz	1	1	1

DC GAIN

DC GAIN	G1	G2
1	1	1
2	1	0
4	0	1
8	0	0

CLOCK TO SCF BANDEDGE DIVIDE DOWN RATIO

fCLK / fc	D0	D1	D2
200	0	0	0
400	0	0	1
800	0	1	0
1,600	0	1	1
3,200	1	0	0
6,400	1	0	1
12,800	1	1	X

DECIMATOR SAMPLE RATE

fS/H / fc	D3	D4
25.000	0	0
12.500	0	1
6.250	1	0
4.167	1	1

fc = 0.1dB bandwidth of the SC filter.
fCLK = Master clock frequency at CLKOUT.
fS/H = Sample rate at SCOUT output.

The SC filter's bandedge is programmed by selecting one of the divide down ratios shown in Table I. This ratio is divided into the master clock frequency to arrive at the filter cutoff frequency. As an example, assuming a typical master clock frequency of 4 MHz and a divide down ratio of 400 (D0, D1, D2=001), the filter's bandedge would be 10 KHz. Alternately, selecting a divide down ratio of 3200 (D0, D1, D2=100) would provide a filter bandedge of 1250Hz. With a constant master clock frequency, up to seven discrete SC filter bandedges can be obtained. An inifinite number of different bandedges can be derived by varying both the divide down ratios and the master clock frequency. This provides the ultimate level in programming flexibility.

For the sidebrazed package, direct microprocessor interface is available: The five control signals, A0, AS, $\overline{\text{WR}}$, $\overline{\text{CS}}$, and DS, allow the user to directly interface to 8-bit microprocessors without additional glue logic. Both Motorola's MPX'ed and non-MPX'ed bus formats as well as Intel's MPX'ed bus format are supported. Interface connections for both the Intel and Motorola 8-bit microprocessors are shown in Table II. In addition to the data-latch format, the D0-D7 and G1-G2 inputs can be hardwired for direct programming without the need for a latch signal by tying the $\overline{\text{CS}}$ input to VSS. A0=1 selects the BW registers D0-D7 and A0=0 selects the gain registers G1, G2.

Table II - Microprocessor Interface Connections

HSCF24040	INTEL (MPX'ED) 8088, 8085, 8051	MOTOROLA (MPX'ED) 6801, 6803	MOTOROLA (NON-MPX'ED) 680D, 6801, 6802, 6809
$\overline{\text{CS}}$	Generated from A8-A15	Generated from A8-A15	Generated from A0-A15
DS	VDD Supply	E	E
$\overline{\text{WR}}$	$\overline{\text{WR}}$	R/$\overline{\text{WR}}$	R/$\overline{\text{WR}}$
A0	ADi	ADi	Ai
AS	ALE	AS	ADD Supply
D0-D7	AD0-AD7	AD0-AD7	D0-D7
G1-G2	ADi	ADi	Di

NOTE: Tying $\overline{\text{CS}}$ to the VSS Supply disables the microprocessor interface and allow D0-D7, G1-G2 to be programmed directly without the need for a latch signal.

OSCILLATOR

The HSCF24040 provides an on-chip oscillator (external crystal) for applications where a system clock is not available. The user has a choice of either the clock driven or oscillator mode. The oscillator mode is enabled by tying the CLKIN input to VSS.

TYPICAL APPLICATION CIRCUIT

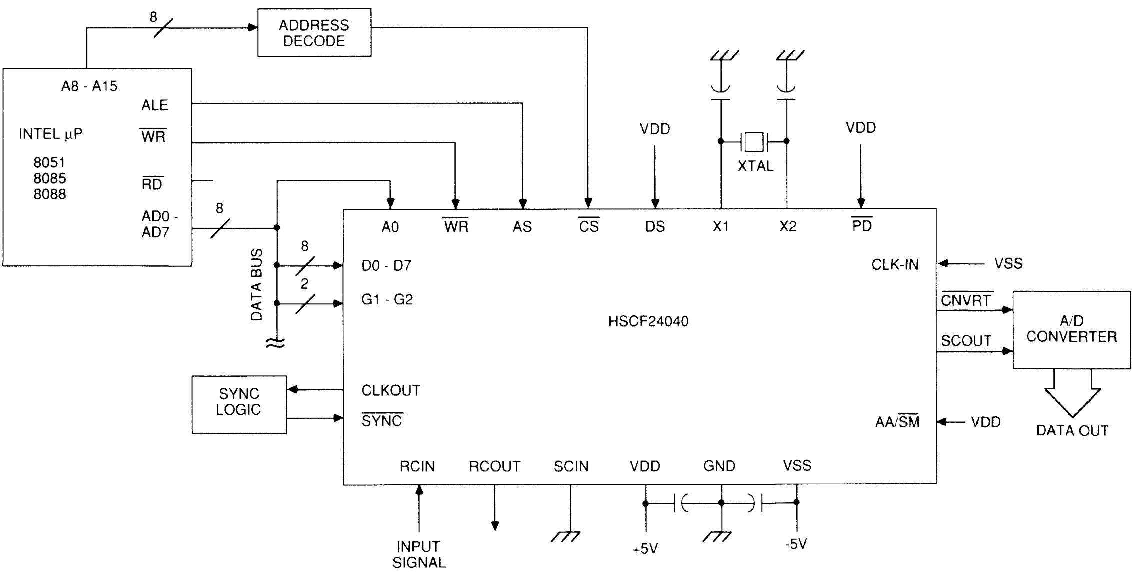
Figure 3 illustrates how the HSCF24040 might be used for smoothing the output from a D/A converter. In this case, the D/A output is fed into the SCIN input of the device. The SCIN input is enabled by tying AA/SM to ground. The SCOUT output is fed externally into the RCIN input. The smoothed output is finally brought off-vhip via the RCOUT pin. (Note that the smoothed output will no correct the inherent sin (X)/(X) droop of the original D/A converter output).

TYPICAL APPLICATION CIRCUIT

The HSCF24040 can be used as the band limiting filter for a 12-bit data acquisition system as shown in Figure 4. The basic function of the device is to bandlimit the input signal so that unwanted, out-of-band signals are not aliased (folded) into the desired passband. The input signal enters the HSCF24040 through RCIN and is processed by the RC filter. The signal is then processed by the switched-capacitor filter, and finally the decimator to facilitate its interface with the A/D converter. Figure 1 shows that for a 12-bit system the filter must provide at least 75 dB of loss at the frequency fs-fc (where fs is the sampling rate of the A/D converter and fc is the desired channel bandwidth).

In many applications the user may want a programmable channel bandwidth. An instrument that records signals that range from 100 Hz to 20 KHz would require that the A/D sample rate be variable. Figure 1 shows that the required filter bandwidth is directly proportional to the sample rate of the A/D converter. The filtering necessary for the multiple sampling rates can be accomplished by using the programmable bandwidth capability of the HSCF24040 to adjust the desired filter response to the sample rate. This eliminates the need for a parallel bank of fixed bandwidth anti-aliasing filters, one for each sample rate.

Figure 3 - The HSCF24040 as an Anti-Aliasing Filter in a 12-bit Data Acquisition System



PIN ASSIGNMENT HSCF24040

TOP VIEW

LCC PACKAGE OPTION

The LCC package function differs from the sidebrazed in that the $\overline{CS}$ pin is internally tied to V_{SS} and pins AO, AS, $\overline{WR}$, and DS are internally tied to ground. D0-D7 and G1-G2 must be programmed directly. External latches may be necessary for microprocessor interfaces. Contact the factory for availability.

PIN FUNCTIONS HSCF24040

NAME	FUNCTION
VSS	Negative supply voltage
$\overline{CS}$	Chip select; active low
G1-G2	The digital inputs that control the DC gain of the SC filter
D0-D7	The digital inputs that control the RC filter bandedge, SC filter bandedge, and SC filter decimation rate.
$\overline{SYNC}$	This digital input conrols the sampling instant for the SC filter decimated output; active low.
CLKOUT	Master clock output capable of driving 1 standard TTL load. It is a buffered version of either CLKIN or the internally generated crystal oscillator output.
VDD	Positive supply voltage
$\overline{CNVRT}$	This digital output indicates that the SCOUT output has settled and can now be deverted or sampled (drive capability is 1 standard TTL load); active low.
X1-X2	An external crystal is connected between these pins to generate an accurate clock for chip operation.
CLKIN	The master clock input. Forcing CLKIN to VSS enables the on-chip oscillator (external crystal).
GND	Ground
SCOUT	SC filter output
$\overline{PD}$	This digital input is used to power down the analog circuitry; active low
RCOUT	RC filter output
RCIN	RC filter input
SCIN	SC filter input (only valid when AA/$\overline{SM}$ is forced low)
$\overline{WR}$	Write strobe; active low
DS	Data strobe
AA/$\overline{SM}$	This digital input controls whether the input to the SC filter comes from RCOUT or SCIN
AS	Address strobe
A0	Register address select

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SPT114

VOLTAGE REGULATOR WITH ON/OFF SWITCH

FEATURES

- Low Dropout Voltage
- Electronic ON/OFF Switch
- Very Low Standby Current (ON, No Load)
- Internal Thermal Shutdown
- Short Circuit Protection
- Very Low (<100 nA) Current in OFF Mode
- Available on Tape and Reel
- Customized Versions Are Available

APPLICATIONS

- Battery Powered Systems
- Cellular Telephones
- Pagers
- Personal Communications Equipment
- Portable Instrumentation
- Portable Consumer Equipment
- Radio Control Systems
- Low Voltage Systems

GENERAL DESCRIPTION

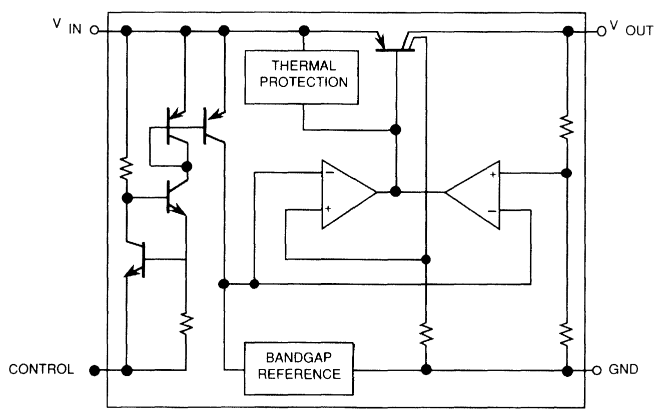
The SPT114 series of devices are low power, linear regulators. Each regulator can be turned ON and OFF by an internal electronic switch which is controlled by an external control signal.

The Internal PNP pass-transistor is used in order to achieve low dropout voltage (typically 200 mV at 50 mA load current). The device has very low quiescent current (500 µA) in the ON mode with no load and 2 mA with 30 mA load. The quiescent current is typically 4 mA at 60 mA load. An internal thermal shutdown circuit limits the junction temperature to below 150 °C. The load current is internally monitored and the device will shut down (no load current) in the presence of a short circuit at the output. The regulated output voltage may be specified in 0.5 V increments between 2.0 to 6.0 V. Additionally, 3.25 V, 4.75 V and 8.0 V versions are also available.

The device is available in a plastic SOT-23L package. Tape and reel mounted devices are also available.

7

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur) 25[1] °C

Supply Voltage .... 14 V
Output Voltage .... V_{OUT} x1.15 V
Load Current .... 180 mA
Power Dissipation (Note 2) .... 200 mW
Storage Temperature Range .... -55 to +150 °C
Operating Temperature Range .... -20 to +75 °C
Lead Soldering Temp (10 sec) .... +240 °C
Junction Temperature .... +150 °C

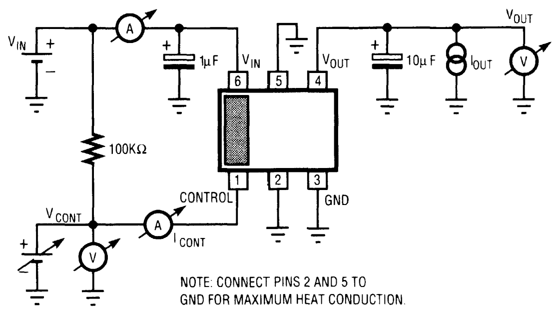
ELECTRICAL SPECIFICATIONS Unless otherwise specified, T_A=25 *C, Note 3

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage Range		V_{IN}	V_{OUT}+1		13	V
Supply Current	I_{OUT}=0 mA, V_{CONT}=0, ON Mode	I_{IN1}		500		µA
Supply Current	V_{CONT}=V_{IN} , OFF Mode	I_{IN2}		0.1	2	µA
Regulated Output Voltage	V_{IN}=V_{OUT} + 1 V, I_{OUT}=10 mA	V_{OUT}	-3.5	V_{OUT}	+3.5	%
Dropout Voltage	I_{OUT}=30 mA	V_{DROP1}		120		mV
Dropout Voltage	I_{OUT}=60 mA	V_{DROP2}		170		mV
Output Current		I_{OUT}	70			mA
Line Regulation	(V_{OUT} + 1.0 V)≤V_{IN}≤V_{OUT}+6.0 V	LI_{REG}		0.04		%/V
Load Regulation	0 mA ≤ I_{OUT}≤60 mA, V_{IN}=V_{OUT} + 1.5 V	LD_{REG}		0.02		%/mA
Ripple Rejection	100 mVRMS, f=400 Hz V_{IN}=V_{OUT} + 1.5 V, I_{OUT}=10 mA	V_{RIPPLE}		55		dB
Output Voltage Temperature Coefficient	0 °C≤T_A≤75 °C, V_{IN}=V_{OUT} + 1.5 V, I_{OUT}=10 mA	$\Delta V_{OUT}/\Delta T_A$		±0.3		mV/°C
Output Noise Voltage	V_{IN}=V_{OUT} + 1.5 V, I_{OUT}=10 mA 10 Hz< f< 100 kHz, I_{OUT}=10 mA	V_N		180		μV_{RMS}

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.
Note 2: Derate above T_A=25 °C at 1.6 mW/°C.
Note 3: Due to the common format used here, some specifications may not apply to all versions of output voltage. Detailed specifications are available for each version.

TYPICAL PERFORMANCE CHARACTERISTICS

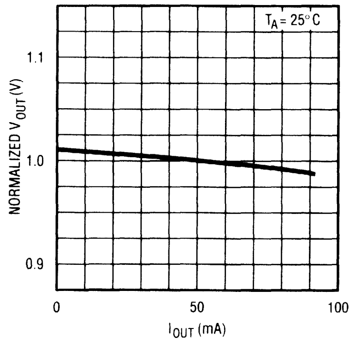
TEST CIRCUIT 1



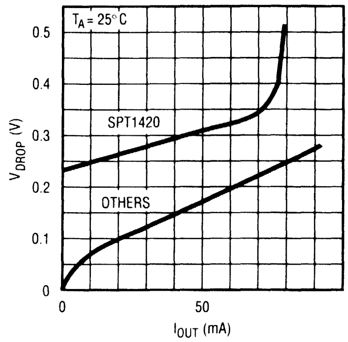
TYPICAL PERFORMANCE CHARACTERISTICS

PART NUMBER	OUTPUT VOLTAGE(V)
SPT11420	2.0
SPT11425	2.5
SPT11430	3.0
SPT11432	3.2
SPT11435	3.5
SPT11440	4.0
SPT11445	4.5
SPT11450	5.0
SPT11455	5.5
SPT11460	6.0
SPT11480	8.0

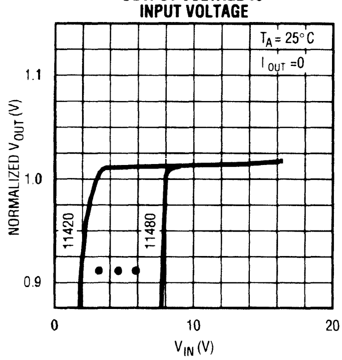
OUTPUT VOLTAGE vs OUTPUT CURRENT



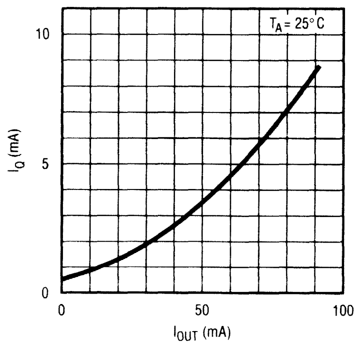
DROPOUT VOLTAGE vs LOAD CURRENT



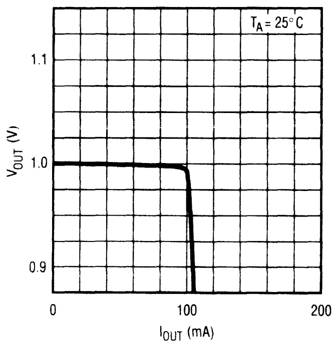
OUTPUT VOLTAGE vs INPUT VOLTAGE



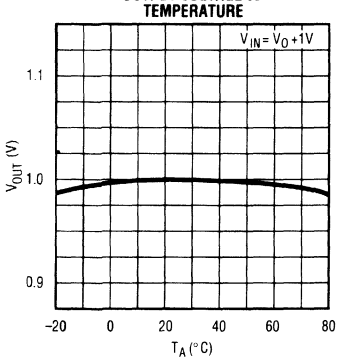
QUIESCENT CURRENT vs LOAD CURRENT



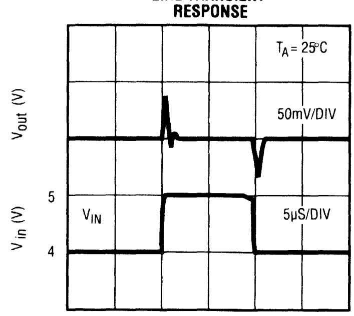
SHORT CIRCUIT PROTECTION



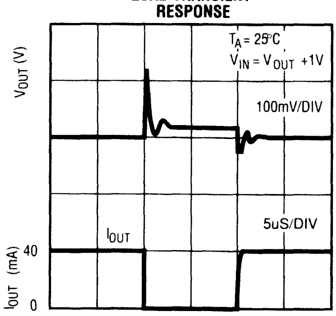
OUTPUT VOLTAGE vs TEMPERATURE



LINE TRANSIENT RESPONSE

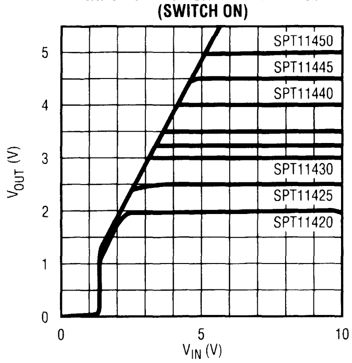


LOAD TRANSIENT RESPONSE

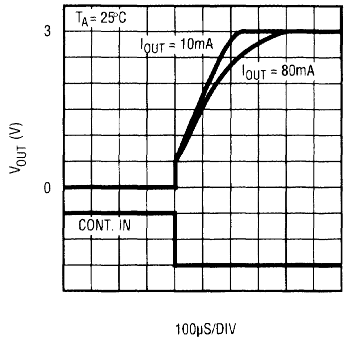


TYPICAL PERFORMANCE CHARACTERISTICS

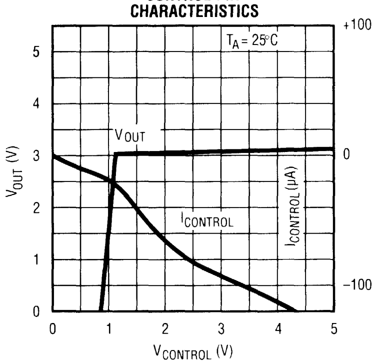
INPUT OUTPUT CHARACTERISTICS (SWITCH ON)



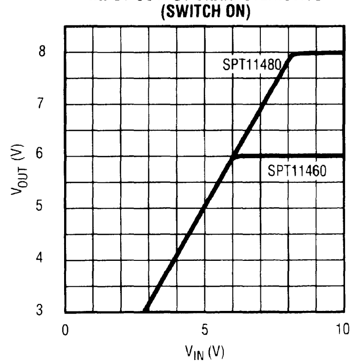
TURN ON TRANSIENT RESPONSE



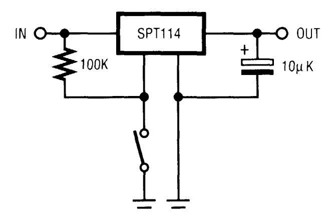
CONTROL PIN CHARACTERISTICS



INPUT OUTPUT CHARACTERISTICS (SWITCH ON)

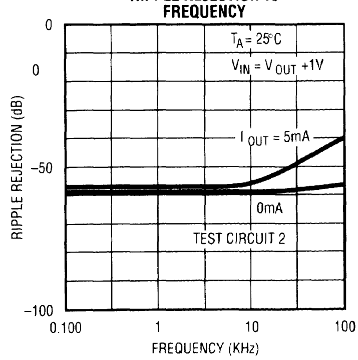


TEST CIRCUIT 2



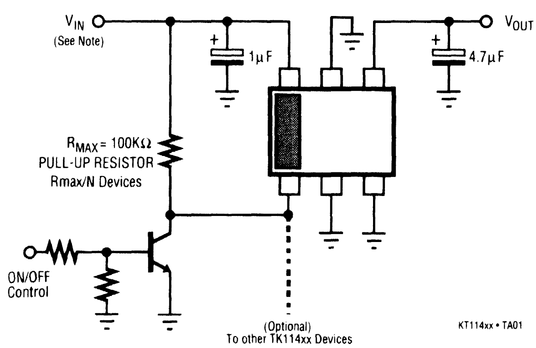
RIPPLE REJECTION TEST CIRCUIT

RIPPLE REJECTION vs FREQUENCY

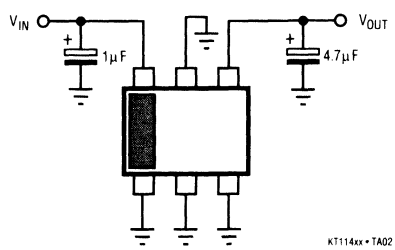


TYPICAL APPLICATIONS

CONTROL FUNCTION UTILIZED

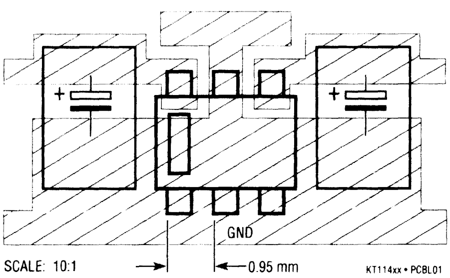


CONTROL FUNCTION NOT UTILIZED



Note: Parallel connection of control pins is allowed if all devices use identical input voltage.

PRINTED CIRCUIT BOARD LAYOUT



APPLICATION HINTS

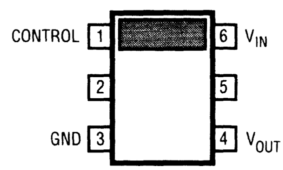
Maximize copper foil area connecting to all IC pins for optimum performance. Place input and output bypass capacitors close to the GND pin. For best transient behavior and lowest output impedance, use as large of a capacitor value as possible. The temperature coefficient of the capacitance and Equivalent Series Resistance (ESR) should be taken into account. These parameters can influence power supply noise and ripple rejection. In extreme cases, oscillation may occur. In order to maintain stability, the output bypass capacitor value should be minimum 2.2 μF in case of Tantalum electrolytic or 4.7 μF in case of Aluminium electrolytic.

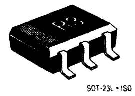
HANDLING MOLDED RESIN PACKAGES

All plastic molded packages absorb some moisture from the air. If moisture absorption occurs prior to soldering the device into the printed circuit board, increased separation of the lead from the plastic molding may occur, degrading the moisture barrier characteristics of the device. This property of plastic molding compounds should not be overlooked, paticularly in the case of very small packages, where the plastic is very thin.

In order to preserve the original moisture barrier properties of the package, devices are stored and shipped in moisture proof bags, filled with dry air. The bags should not be opened or damaged prior to the actual use of the devices. If this is unavoidable, the devices should be stored in a low relative humidity environment (40 to 65%) or in an enclosed environment with desicant.

PIN ASSIGNMENT





SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

SPT115

VOLTAGE REGULATOR WITH ON/OFF SWITCH

FEATURES

- Low Noise and Dropout Voltage
- Pass Transistor Terminals Available
- Very Low Standby Current (ON, No Load)
- Very Low (<100 nA) Current in OFF Mode
- Small Outline Surface Mount Package
- Internal Thermal Shutdown
- Short Circuit Protection
- Available on Tape and Reel
- Customized Versions Are Available

APPLICATIONS

- Cordless Telephones
- Pagers
- Battery Powered Systems
- Personal Communications Equipment
- Portable Instrumentation
- Radio Control Systems
- Low Voltage Systems
- Portable Consumer Equipment

GENERAL DESCRIPTION

The SPT115 series devices are low power, linear regulators with electronic ON/OFF switches. Both active HIGH and active LOW control pins are provided.

An internal PNP pass-transistor is used in order to achieve low dropout voltage (typically 200 mV at 80 mA load current). The base of the internal pass transistor is available at pin 7 for parallel connection of an external pass transistor in case higher current or lower dropout voltage is required.

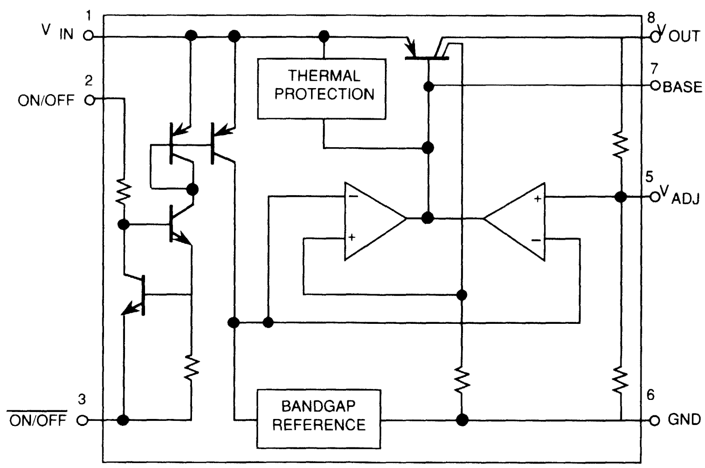
The regulated output voltage may be specified in 0.5 V increments between 2.5 to 5.5 V. Additionally, 3.2 V, 4.7 V and 8 V output versions are also available.

The devices operate at very low (500 µA) quiescent current with no load, 2 mA with 40 mA load, and 3 mA with 60 mA load. An internal thermal shutdown circuit limits the junction temperature to below 150 °C. The load current is internally monitored, and the device will shut down in the presence of a short circuit at the output.

The SPT115 is available in an 8-lead plastic surface mount package. Tape and reel mounted devices are also available.

7

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltage .... 14 V
Output Voltage .... V_{OUT} x1.15 V
Load Current .... 180 mA
Power Dissipation (Note 2) .... 600 mW

Storage Temperature Range .... -55 to +150 °C
Operating Temperature Range .... -20 to +75 °C
Lead Soldering Temp (10 sec) .... +260 °C
Junction Temperature .... +150 °C

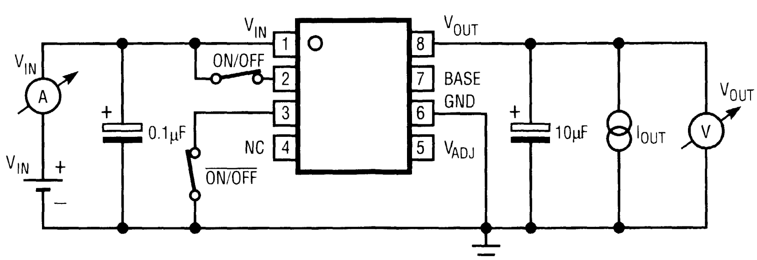
ELECTRICAL SPECIFICATIONS Unless otherwise specified, T_A=25 °C, Note 3

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Current	I_{OUT}=0 mA, ON Mode	I_{IN1}		500		µA
Supply Current	OFF Mode	I_{IN2}		0.1	2	µA
Regulated Output Voltage	$V_{IN}=V_{OUT}$ + 1 V, I_{OUT}=30 mA Note 3	V_{OUT}	-3.0	V_{OUT}	+3.0	%
Dropout Voltage	I_{OUT}=60 mA	V_{DROP}		170		mV
Output Current		I_{OUT}	100			mA
Line Regulation	(V_{OUT} + 1.0 V)≤V_{IN}≤V_{OUT}+6.0 V	LI_{REG}		0.02		%/V
Load Regulation	0 mA ≤ I_{OUT}≤60 mA, $V_{IN}=V_{OUT}$ + 1.0 V	LD_{REG}		0.01		%/mA
Ripple Rejection	100 mVRMS, f=400 Hz $V_{IN}=V_{OUT}$ + 1.5 V, I_{OUT}=10 mA	V_{RIPPLE}		55		dB
Output Voltage Temperature Coefficient	0 °C≤T_A≤75 °C, $V_{IN}=V_{OUT}$ + 1.5 V, I_{OUT}=10 mA	$\Delta V_{OUT}/\Delta T_A$		±0.3		mV/°C
Output Noise Voltage	$V_{IN}=V_{OUT}$ + 1.5 V, I_{OUT}=10 mA 10 Hz< f< 100 kHz	V_N		180		µV_{RMS}

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.
Note 2: Derate above T_A=25 °C at 4.8 mW/°C.
Note 3: Due to the common format used here, some specifications may not apply to all versions of output voltage. Example: V_{OUT} tolerance is ±4% for SPT11520, STP11525 and SPT11530. Detailed specifications are available for each version.

TYPICAL PERFORMANCE CHARACTERISTICS AT 25 °C

TEST CIRCUIT 1

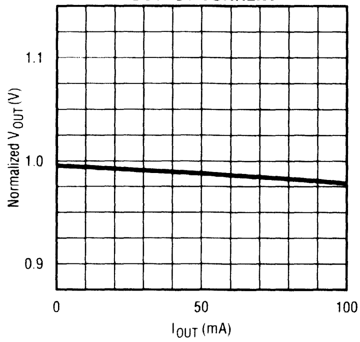


TYPICAL PERFORMANCE CHARACTERISTICS AT 25 °C

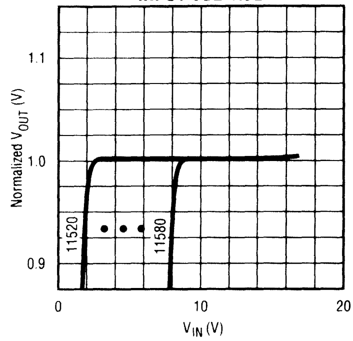
GRAPHS ASSOCIATED WITH TEST CIRCUIT 1

PART NUMBER	OUTPUT VOLTAGE(V)
SPT11520	2.0
SPT11525	2.5
SPT11530	3.0
SPT11532	3.2
SPT11535	3.5
SPT11540	4.0
SPT11545	4.5
SPT11547	4.7
SPT11550	5.0
SPT11555	5.5
SPT11580	8.0

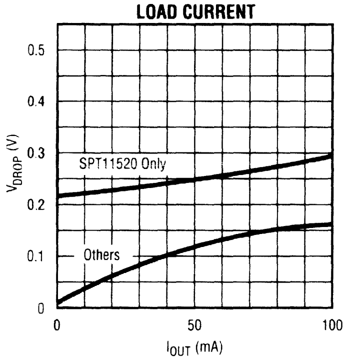
OUTPUT VOLTAGE vs OUTPUT CURRENT



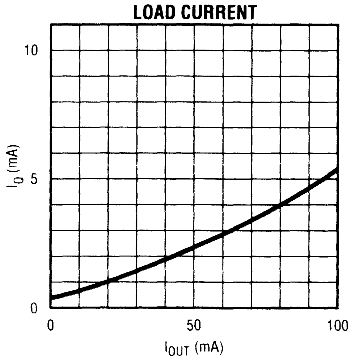
OUTPUT VOLTAGE vs INPUT VOLTAGE



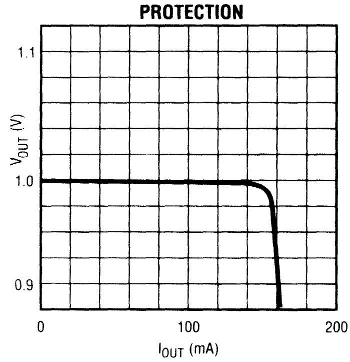
DROPOUT VOLTAGE vs LOAD CURRENT



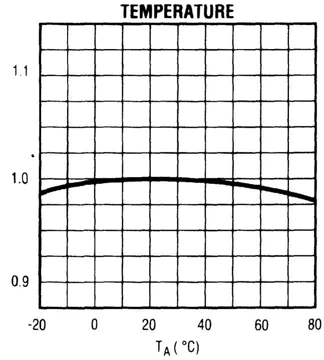
QUIESCENT CURRENT vs LOAD CURRENT



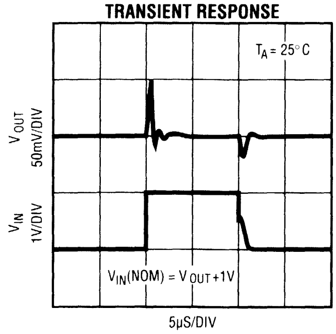
SHORT CIRCUIT PROTECTION



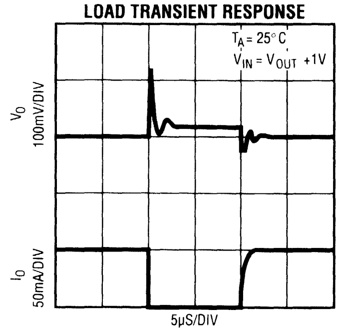
OUTPUT VOLTAGE vs TEMPERATURE



LINE TRANSIENT RESPONSE



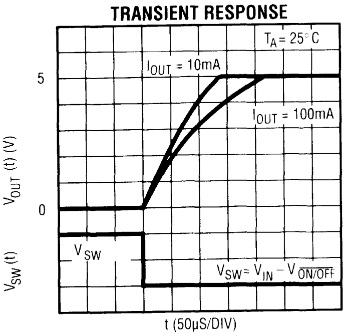
LOAD TRANSIENT RESPONSE



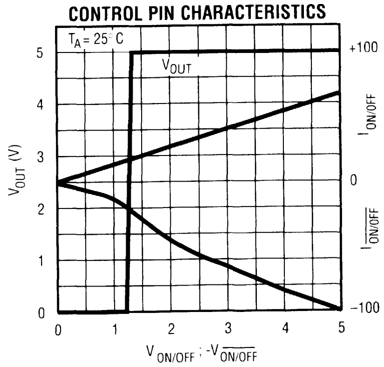
7

TYPICAL PERFORMANCE CHARACTERISTICS AT 25 °C

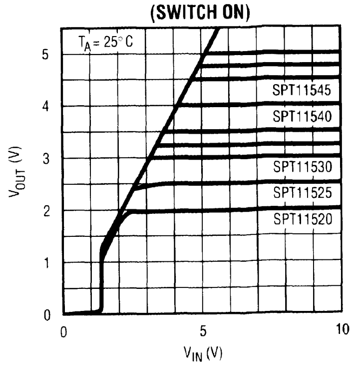
TURN ON TRANSIENT RESPONSE



CONTROL PIN CHARACTERISTICS

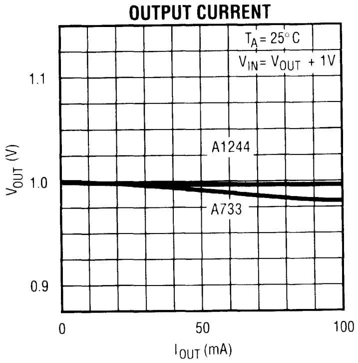


INPUT OUTPUT CHARACTERISTICS (SWITCH ON)

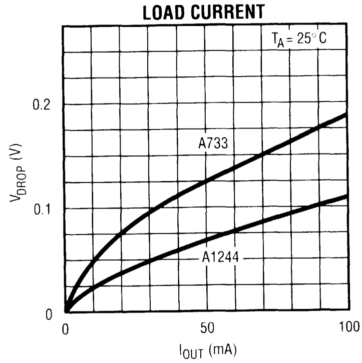


COMMON CHARACTERISTICS OF THE SPT11550 WITH EXTERNAL CURRENT BOOST TRANSISTOR (NEC 2SA733 OR TOSHIBA 2SA1244). SEE TYPICAL APPLICATIONS CIRCUIT ENTITLED ACTIVE HIGH CONTROL WITH CURRENT BOOST.

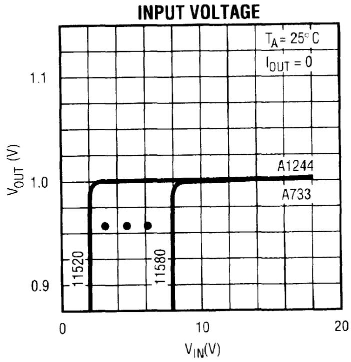
OUTPUT VOLTAGE vs OUTPUT CURRENT



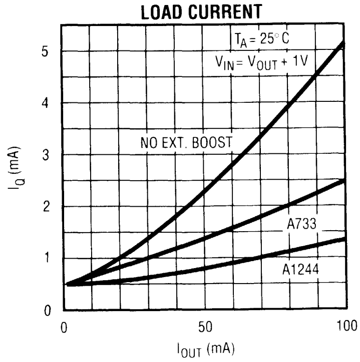
DROPOUT VOLTAGE vs LOAD CURRENT



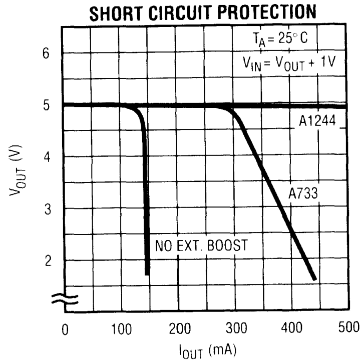
OUTPUT VOLTAGE vs INPUT VOLTAGE



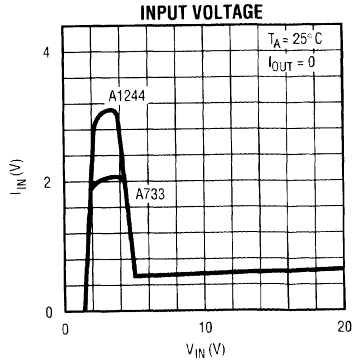
QUIESCENT CURRENT vs LOAD CURRENT



SHORT CIRCUIT PROTECTION



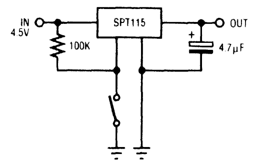
INPUT CURRENT vs INPUT VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS AT 25 °C

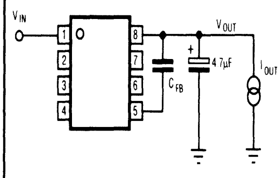
ADDITIONAL TEST CIRCUITS AND ASSOCIATED GRAPHS

TEST CIRCUIT 2



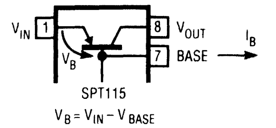
RIPPLE REJECTION TEST

TEST CIRCUIT 3



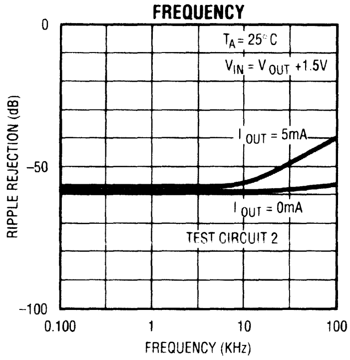
NOISE LEVEL TEST CIRCUIT

TEST CIRCUIT 4

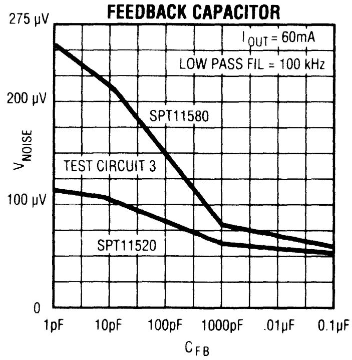


INTERNAL PASS TRANSISTOR

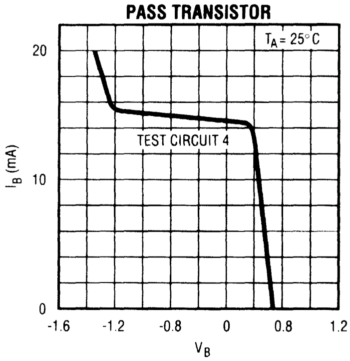
RIPPLE REJECTION vs FREQUENCY



NOISE LEVEL vs FEEDBACK CAPACITOR



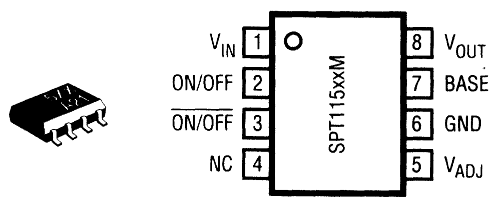
INTERNAL PASS TRANSISTOR



APPLICATION HINTS

Maximize copper foil area connecting to all IC pins for optimum performance. Place input and output bypass capacitors close to the GND pin. For best transient behavior and lowest output impedance, use as large of a capacitor value as possible. The temperature coefficient of the capacitance and Equivalent Series Resistance (ESR) should be taken into account. These parameters can influence power supply noise and ripple rejection. In extreme cases, oscillation may occur. In order to maintain stability, the output bypass capacitor value should be minimum 1 µF in case of Tantalum electrolytic or 4.7 µF in case of Aluminium electrolytic at T_A = 25 °C.

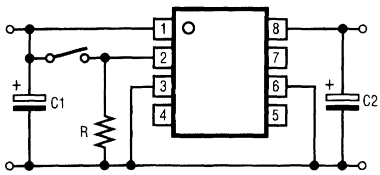
PIN ASSIGNMENTS



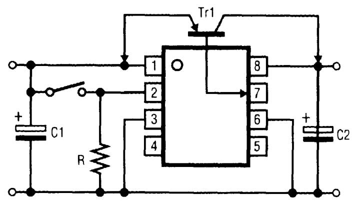
KT115xxM • PO

TYPICAL APPLICATIONS

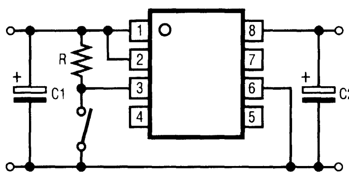
ACTIVE HIGH CONTROL



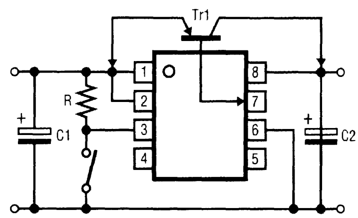
ACTIVE HIGH CONTROL WITH CURRENT BOOST



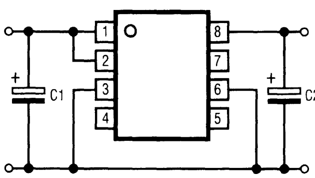
ACTIVE LOW CONTROL



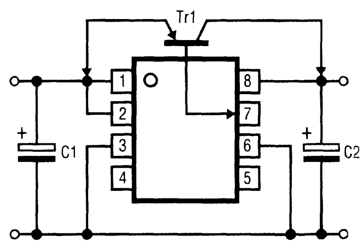
ACTIVE LOW CONTROL WITH CURRENT BOOST



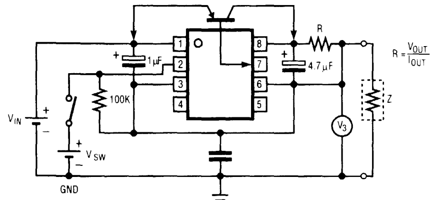
NO SWITCH CONTROL



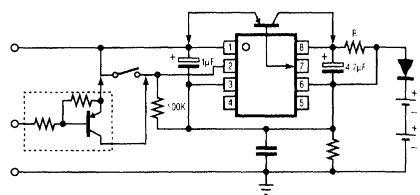
NO SWITCH CONTROL WITH CURRENT BOOST



CURRENT MODE REGULATOR WITH "ON/OFF" CONTROL AND CURRENT BOOST



BATTERY CHARGER WITH "ON/OFF" CONTROL AND CURRENT BOOST



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7

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN
DATA CONVERSION
AND
SIGNAL PROCESSING

SPT

SIGNAL PROCESSING TECHNOLOGIES

SPT116

THREE TERMINAL VOLTAGE REGULATOR

FEATURES

- Low Dropout Voltage
- Very Low Standby Current (No Load)
- Good Load Regulation
- Internal Thermal Shutdown
- Short Circuit Protection
- 3% Output Voltage Accuracy
- Available On Paper Tape
- Customized Versions Are Available

APPLICATIONS

- Battery Powered Systems
- Portable Consumer Equipment
- Cordless Telephones
- Personal Communications Equipment
- Portable Instrumentation
- Radio Control Systems
- Low Voltage Systems

GENERAL DESCRIPTION

The SPT116 series devices are low power, linear 3-terminal regulators.

An internal PNP pass-transistor is used in order to achieve low dropout voltage (typically 200 mV at 80 mA load current).

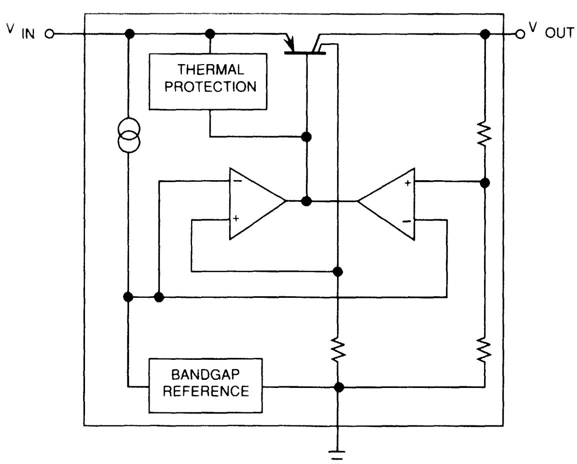
The regulated output voltage may be specified in 0.5 V increments between 2.0 to 5.5 V. The device has very low (400 μA) quiescent current with no load and 2 mA with 60 mA load.

An internal thermal shutdown circuit limits the junction temperature to below 150 °C. The load current is internally monitored and the device will shut down in the presence of a short circuit at the output.

The SPT116 series is available in plastic TO-92N and plastic tape and reel TO-92NT packages.

7

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltage .... 16 V
Output Voltage .... V_{OUT} x1.15 V
Load Current .... 180 mA
Power Dissipation (Note 2) .... 500 mW

Storage Temperature Range .... -55 to +150 °C
Operating Temperature Range .... -20 to +75 °C
Lead Soldering Temp (10 sec) .... +260 °C
Junction Temperature .... +150 °C

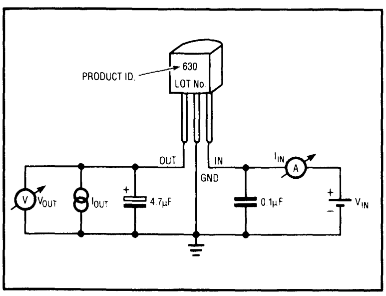
ELECTRICAL SPECIFICATIONS Unless otherwise specified, T_A=25 °C, Note 3

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage Range		V_{IN}	V_{OUT}+1		14	V
Supply Current	I_{OUT}=0 mA	I_{IN1}		400		µA
Supply Current	V_{IN}=V_{OUT}	I_{IN2}		800		µA
Regulated Output Voltage	V_{IN}=V_{OUT} + 1 V, I_{OUT}=10 mA	V_{OUT}	-3.0	V_{OUT}	+3.0	%
Dropout Voltage	I_{OUT}=0 mA	V_{DROP1}		50		mV
Dropout Voltage	I_{OUT}=60 mA	V_{DROP2}		170		mV
Output Current		I_{OUT}	100			mA
Line Regulation	(V_{OUT} + 1.0 V) ≤V_{IN}≤(V_{OUT}+6.0 V)	LI_{REG}		0.01		%/V
Load Regulation	0 mA ≤ I_{OUT}≤30 mA, V_{IN}=V_{OUT} + 1.0 V	LD_{REG1}		0.02		%/mA
Load Regulation	0 mA ≤ I_{OUT}≤60 mA, V_{IN}=V_{OUT} + 1.0 V	LD_{REG2}		0.03		%/mA
Ripple Rejection	100 mV_{RMS}, f=400 Hz V_{IN}=V_{OUT} + 1.5 V, I_{OUT}=10 mA	V_{RIPPLE}		55		dB
Output Voltage Temperature Coefficient	0 °C≤T_A≤75 °C, V_{IN}=V_{OUT} + 1.5 V, I_{OUT}=10 mA	$\Delta V_{OUT}/\Delta T_A$		±0.2		mV/°C
Output Noise Voltage	V_{IN}=V_{OUT} + 1.5 V, I_{OUT}=10 mA 10 Hz< f< 100 kHz, I_{OUT}=10 mA	V_N		150		μV_{RMS}

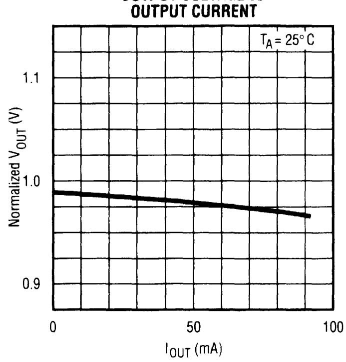
Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.
Note 2: Derate above T_A=25 °C at 1.6 mW/°C.
Note 3: Due to the common format used here, some specifications may not apply to all versions of output voltage. Example: V_{OUT} tolerance is ±4% of SPT11520, STP11525 and SPT11530. Detailed specifications are available for each version.

TYPICAL PERFORMANCE CHARACTERISTICS

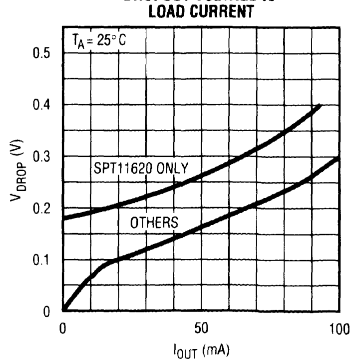
TEST CIRCUIT 1



OUTPUT VOLTAGE vs OUTPUT CURRENT

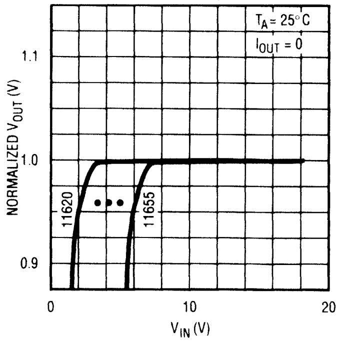


DROPOUT VOLTAGE vs LOAD CURRENT

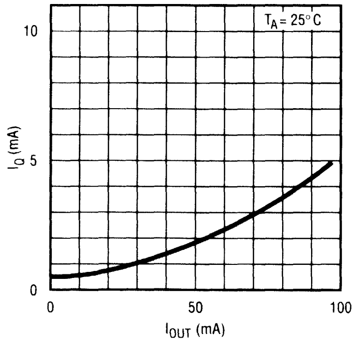


TYPICAL PERFORMANCE CHARACTERISTICS

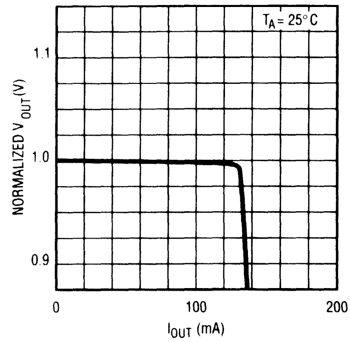
OUTPUT VOLTAGE vs INPUT VOLTAGE



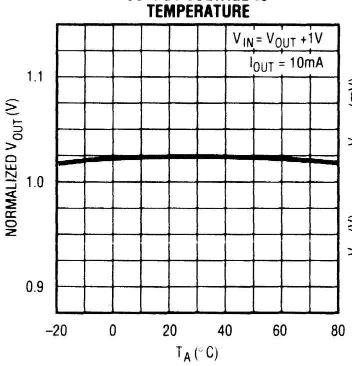
QUIESCENT CURRENT vs LOAD CURRENT



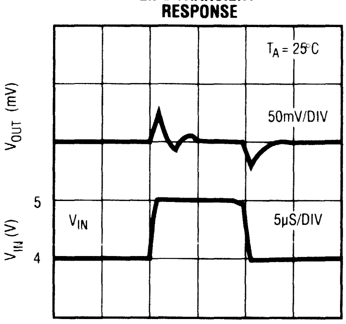
SHORT CIRCUIT PROTECTION



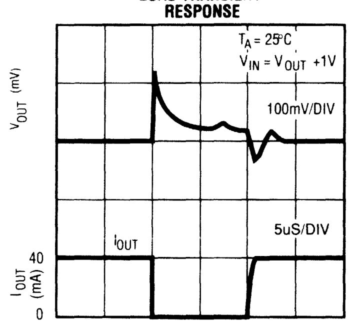
OUTPUT VOLTAGE vs TEMPERATURE



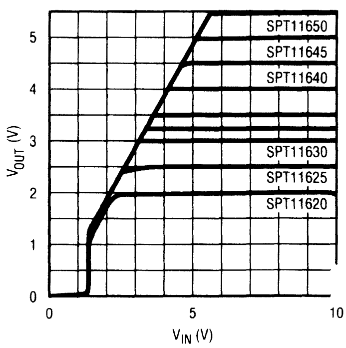
LINE TRANSIENT RESPONSE



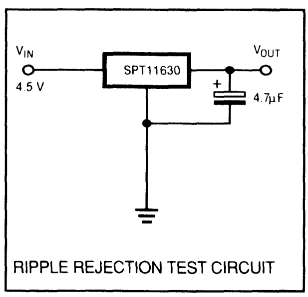
LOAD TRANSIENT RESPONSE



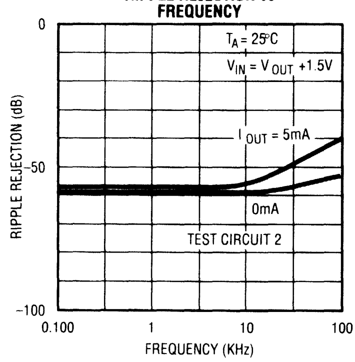
INPUT OUTPUT CHARACTERISTICS



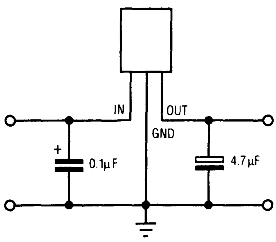
TEST CIRCUIT 2



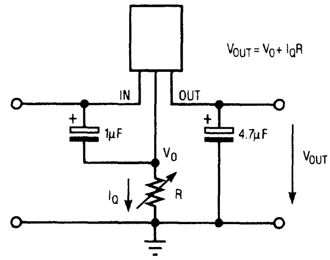
RIPPLE REJECTION vs FREQUENCY



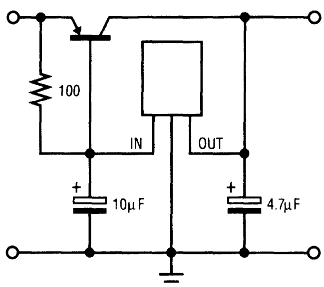
VOLTAGE REGULATOR CIRCUIT



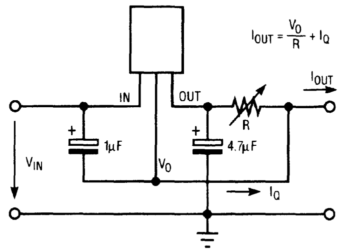
VOLTAGE BOOST CIRCUIT



CURRENT BOOST CIRCUIT



CURRENT REGULATOR CIRCUIT



APPLICATION HINTS

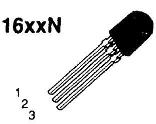
Maximize copper foil area connecting to all IC pins for optimum heat conduction. Place input and output bypass capacitors close to the GND pin.

For best transient behavior and lowest output impedance, use as large of a capacitor value as possible. The temperature coefficient of the capacitance and Equivalent Series Resistance (ESR) should be taken into account. These parameters can influence power supply noise and ripple rejection. In extreme cases, oscillation may occur. In order to maintain stability, the output bypass capacitor value should be minimum 1 µF in case of Tantalum electrolytic or 4.7 µF in case of Aluminium electrolytic at T_A=25 °C.

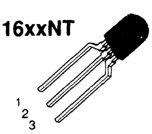
PART NUMBER	OUTPUT VOLTAGE(V)
SPT11620	2.0
SPT11625	2.5
SPT11630	3.0
SPT11632	3.2
SPT11635	3.5
SPT11640	4.0
SPT11645	4.5
SPT11650	5.0
SPT11655	5.5

PIN ASSIGNMENTS

SPT116xxN



SPT116xxNT



PIN 1. OUTPUT
2. GROUND
3. INPUT

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SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SPT11806

DC-DC CONVERTER

SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- Very Small Size
- Few External Components
- Wide Input Supply Voltage Range (1.1 to 18 V)
- Six Selectable Output Voltages up to 32 V
- Single Battery Cell Operation

APPLICATIONS

- Variable Capacitance and PIN Photodiode Bias
- Portable Instrumentation
- Radio Control Systems
- Mobile Radios
- Cellular Telephones
- Cordless Telephones
- Fiber-optic Receivers
- Local Area Network (LAN) Receivers
- Battery Operated Equipment

GENERAL DESCRIPTION

The SPT11806 is a low power, low input voltage DC-DC converter.

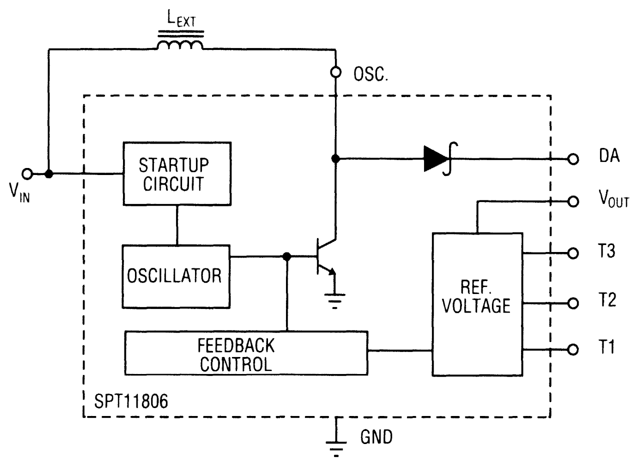
The device has been optimized for variable capacitance diode and PIN diode bias applications. It generates DC output voltages ranging from 9.3 V to 32 V in six steps. The desired output voltage may be selected by simple wire connections between control pins. The input DC voltage can be as low as 1.1 V or as high as 18 V.

The device has a built-in relaxation oscillator. The frequency of oscillation is determined by external component values. The SPT11806 has built-in voltage reference and an array of temperature compensated zener diodes in order to generate various output voltages with minimum external part count.

The device is available in an 8-lead plastic surface mount package (MFP-8) or a 10-lead plastic (ZP-10) package.

8

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Input Voltage, V_{IN} .... 20 V
Output Voltage, V_{OUT} .... 35 V
Power Dissipation SPT11806M (Note2) .... 350 mW
Power Dissipation SPT11806Z (Note3) .... 490 mW
Junction Temperature. .... 150 °C

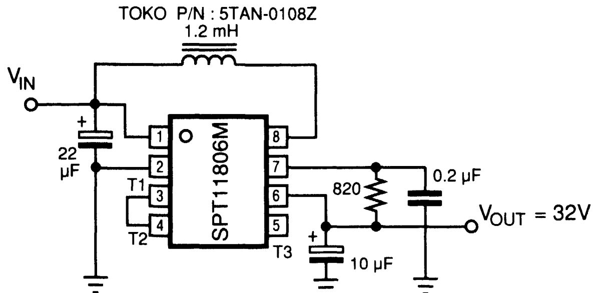
Storage Temperature Range .... -55 to +150 °C
Operating Temperature Range .... -20 to +75 °C
Lead Soldering Temp. (10sec.) M-Package .... 260 °C
Lead Soldering Temp. (10sec.) Z-Package .... 300 °C

ELECTRICAL SPECIFICATIONS V_{IN}=5.0 V, V_{OUT}=32.0 V unless otherwise specified. T_A=25 °C

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage Range		V_{IN}	1.1		18	V
Input Current	V_{OUT}=32 V, I_{OUT}=0.1 mA	I_{IN}		4.7	9	mA
Input Current	V_{OUT}=32 V, I_{OUT}=1.0 mA	I_{IN}		12.1	19	mA
Output Voltage[4]	I_{OUT}=0 µA, 1.1 V≤V_{IN}≤18.0 V	V_{OUT1}	30	32	34	V
Output Voltage[4]	I_{OUT}=0 µA, 1. 1V≤V_{IN}≤18. 0V	V_{OUT2}	26	28	30	V
Output Voltage[4]	I_{OUT}=0 µA, 1.1 V≤V_{IN}≤18. 0V	V_{OUT3}	22	24	26	V
Output Voltage[4]	I_{OUT}=0 µA, 1. 1V≤V_{IN}≤15. 0V	V_{OUT4}	15.5	16.8	18	V
Output Voltage[4]	I_{OUT}=0 µA, 1.1 V≤V_{IN}≤11. 0V	V_{OUT5}	11	12.8	14.5	V
Output Voltage[4]	I_{OUT}=0 µA, 1.1 V≤V_{IN}≤8. 0V	V_{OUT6}	8	9.3	10.5	V
Output Current[5]	V_{OUT}=32 V	I_{OUT}	1.8	2.4		mA
Load Regulation	0.0 mA≤I_{OUT}≤1.0 mA	LD_{REG}		0.24	0.5	%
Temperature Coefficient	V_{OUT}=32 V, I_{OUT}=0.1 mA	$\Delta V_{OUT1}/\Delta T_A$		0.25		mV/°C
Oscillator Start-up Voltage	I_{OUT}=0 mA	V_{OSC}		0.9	1.1	V

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
Note 2: Derate above T_A=25 °C at 3 mW/°C
Note 3: Derate above T_A=25 °C at 4.5 mW/°C
Note 4: Connect T_1 through T_3 as specified.
Note 5: Use inductor as specified.

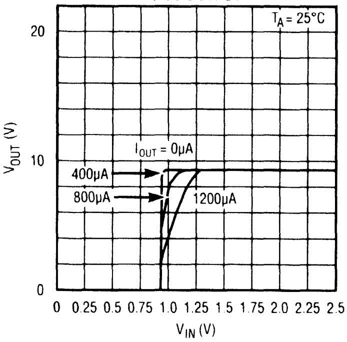
TEST CIRCUIT 1



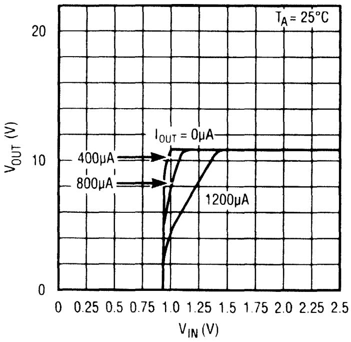
OUTPUT VOLTAGE (V)	CONNECTION
32	T_1-T_2
28	T_1-T_3
24	T_1-T_2-T_3
17	T_1-T_2, T_3-V_{OUT}
13	T_1-V_{OUT}
9.3	T_1-T_2-V_{OUT}

TYPICAL PERFORMANCE CHARACTERISTICS

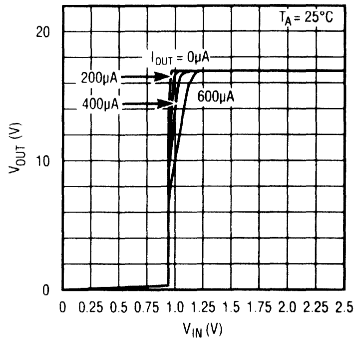
OUTPUT VOLTAGE vs INPUT VOLTAGE 9.3V OUTPUT



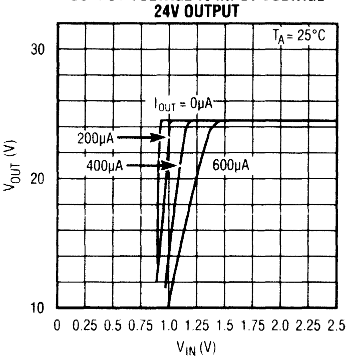
OUTPUT VOLTAGE vs INPUT VOLTAGE 13V OUTPUT



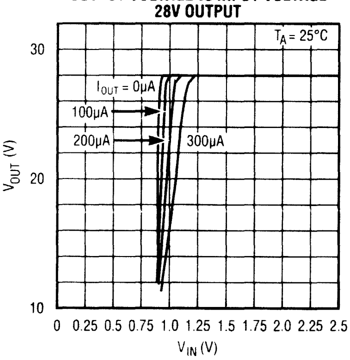
OUTPUT VOLTAGE vs INPUT VOLTAGE 17V OUTPUT



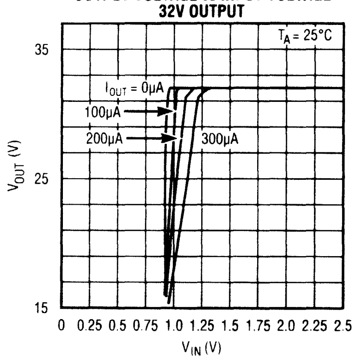
OUTPUT VOLTAGE vs INPUT VOLTAGE 24V OUTPUT



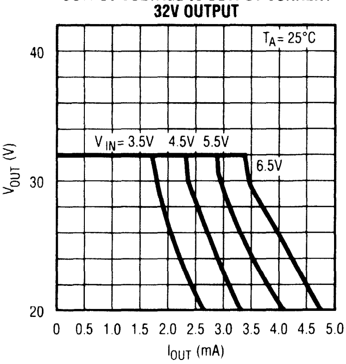
OUTPUT VOLTAGE vs INPUT VOLTAGE 28V OUTPUT



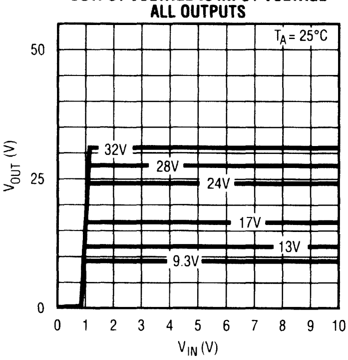
OUTPUT VOLTAGE vs INPUT VOLTAGE 32V OUTPUT



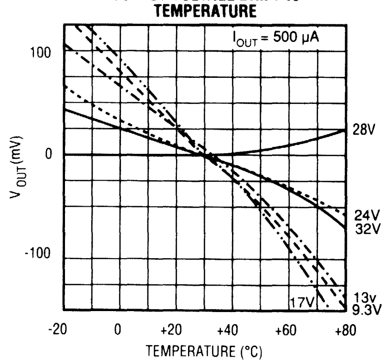
OUTPUT VOLTAGE vs OUTPUT CURRENT 32V OUTPUT



OUTPUT VOLTAGE vs INPUT VOLTAGE ALL OUTPUTS



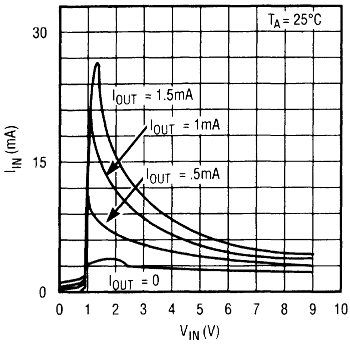
OUTPUT VOLTAGE DRIFT vs TEMPERATURE



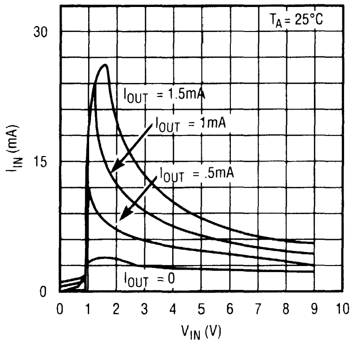
8

TYPICAL PERFORMANCE CHARACTERISTICS

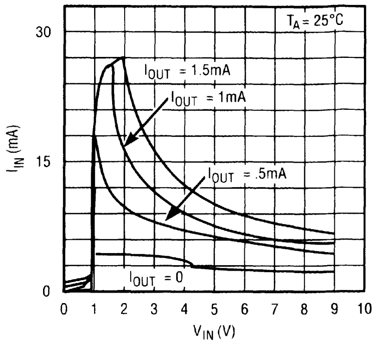
INPUT CURRENT vs INPUT VOLTAGE 9.3V OUTPUT



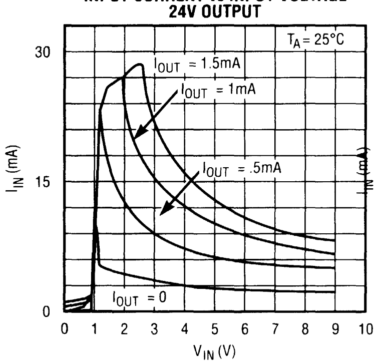
INPUT CURRENT vs INPUT VOLTAGE 13V OUTPUT



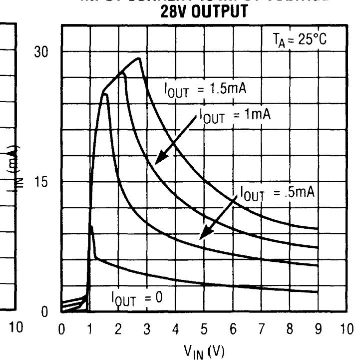
INPUT CURRENT vs INPUT VOLTAGE 17V OUTPUT



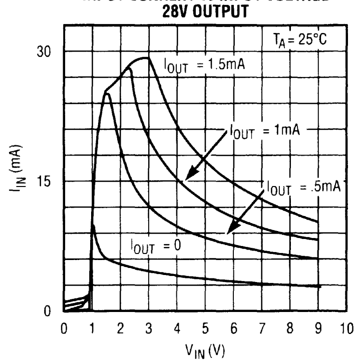
INPUT CURRENT vs INPUT VOLTAGE 24V OUTPUT



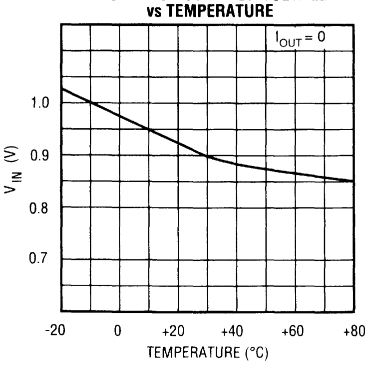
INPUT CURRENT vs INPUT VOLTAGE 28V OUTPUT



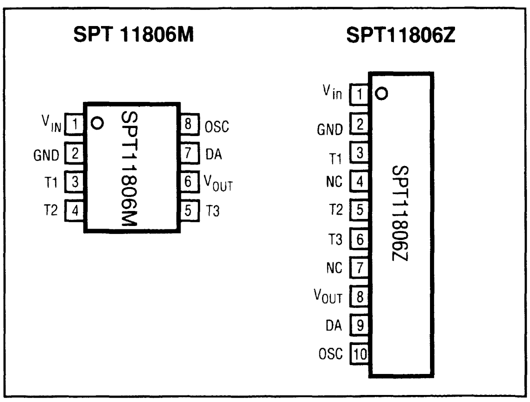
INPUT CURRENT vs INPUT VOLTAGE 28V OUTPUT



OSCILLATOR START-UP VOLTAGE vs TEMPERATURE

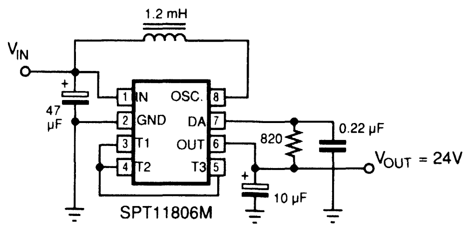


PIN ASSIGNMENT

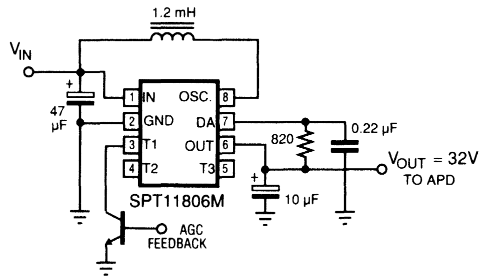


TYPICAL APPLICATIONS

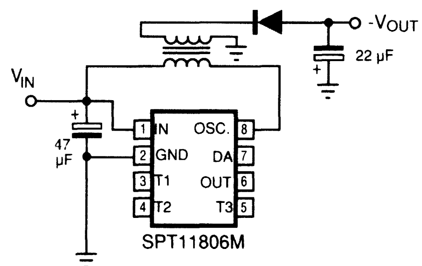
VARIABLE CAPACITANCE DIODE BIAS CIRCUIT



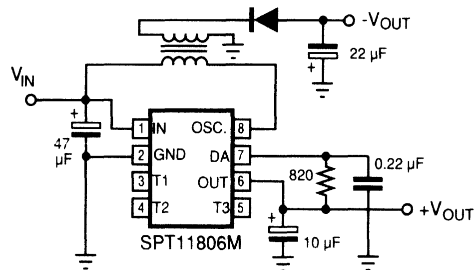
AVALANCHE PHOTODIODE BIAS WITH AGC



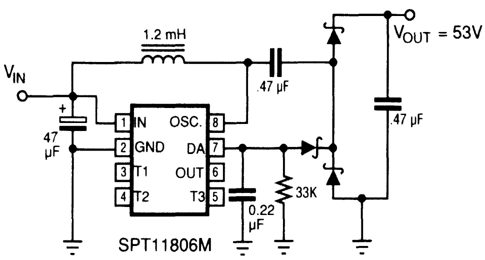
NEGATIVE OUTPUT



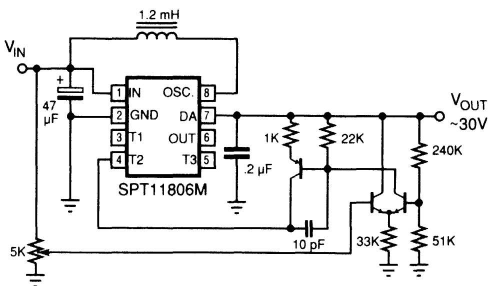
POSITIVE AND NEGATIVE OUTPUTS



VOLTAGE BOOST CIRCUIT



VARIABLE BIAS SOURCE



SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN
DATA CONVERSION
AND
SIGNAL PROCESSING

SPT

SIGNAL PROCESSING TECHNOLOGIES

SPT11821

DC-DC CONVERTER

FEATURES

- Very Low Noise
- Very Small Size
- Few External Components
- Wide Supply Voltage Range (0.9 to 10 V)
- Sinewave Oscillator
- Selectable Output Voltages

APPLICATIONS

- Variable Capacitance and PIN Photodiode Bias
- Portable Instrumentation
- Radio Control Systems
- Mobile Radios
- Cellular Telephones
- Cordless Telephones
- Fiber-optic Receivers
- Local Area Network (LAN) Receivers
- Battery Operated Equipment

GENERAL DESCRIPTION

The SPT11821 is a low power, low input voltage DC-DC converter. The device has been optimized for variable capacitance diode and PIN photodiode bias applications. It generates 10 Vdc and 24 Vdc output voltages from an input voltage as low as 0.9 V.

Since the built-in high frequency oscillator generates sinewaves, the SPT11821 produces very low RF interference noise. The internal oscillator is capable of operation at frequencies as high as 6-8 MHz, therefore, interference filtering is simple and effective. This unique feature makes the SPT11821 ideally suitable for RF and fiber optic receiver applications.

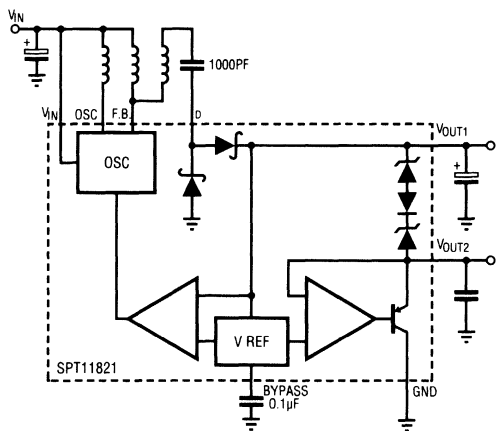
The device is capable of operation in the 0.9 to 10 V power supply voltage range.

Output 1 provides 24 V output, while Output 2 is at 10 V. When Output 1 and Output 2 are shorted, 10 V is available.

The SPT11821 is available in 8-pin plastic surface mount (MFP-8) and 10-pin plastic (ZP-10) packages.

8

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Input Voltage, V_{IN} .... 10 V
Power Dissipation SPT11821M (Note2) .... 350 mW
Power Dissipation SPT11821Z (Note3) .... 490 mW
Junction Temperature .... 150 °C

Storage Temperature Range .... -55 to +150 °C
Operating Temperature Range .... -20 to +75 °C
Lead Soldering Temp. (10 sec.) M-Package .... 260 °C
Lead Soldering Temp. (10 sec.) Z-Package .... 300 °C

ELECTRICAL SPECIFICATIONS V_{IN}=1.1 V; Unless otherwise specified. T_A=25 °C

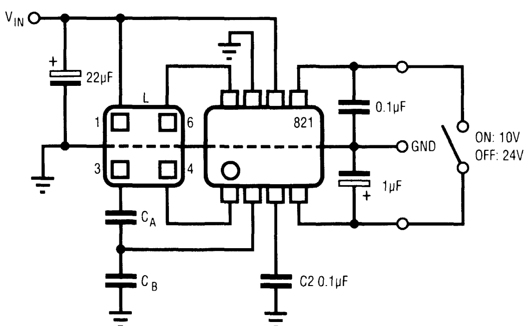
PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Input Voltage	C_A=33 pF, C_B=10 pF	V_{IN1}	0.9		2.0	V
Input Voltage	C_A=820 pF, C_B=33 pF	I_{IN2}	1.8		10	V
Input Voltage	I_{OUT}=0 µA, V_{OUT}=10 V	I_{IN1}		3.5	7	mA
Input Voltage	I_{OUT}=50 µA, V_{OUT}=10 V	I_{IN2}		5.5	9	mA
Output Voltage	I_{OUT}=50 µA	V_{OUT1}	22.5	24.0	25.5	V
Output Voltage	I_{OUT}=50 µA, V_{OUT1} and V_{OUT2} shorted	V_{OUT2}	9.6	10.0	10.4	V
OutputCurrent	V_{OUT1} and V_{OUT2} shorted	I_{OUT}	90.0	100		µA
Temperature Coefficient	V_{OUT1} =24V, I_{OUT1}=50 µA	$\Delta V_{OUT1} / \Delta T_A$		+2.3		mV/°C
Temperature Coefficient	V_{OUT2} =10V, I_{OUT2}=5 0µA	$\Delta V_{OUT2} / \Delta T_A$		-1.5		mV/°C
Oscillator Start-up Voltage	I_{OUT}= 0 µA	V_{START}	0.75			V
Oscillator Frequency	I_{OUT}= 0 µA	f_{OSC}		4		MHz

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

Note 2: Derate above T_A=25 °C at 3 mW/°C
Note 3: Derate above T_A=25 °C at 4 mW/°C

TYPICAL PERFORMANCE CHARACTERISTICS

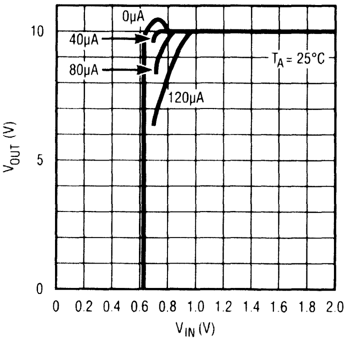
TEST CIRCUIT 1



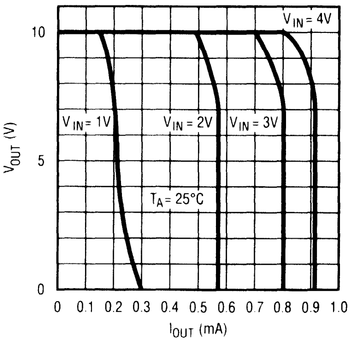
INPUT VOLTAGE	C_A	C_B	TOKO COIL PART NUMBER	OSCILLATOR FREQUENCY
0.9 V to 2 V	33 pF	10 pF	PS5CDLN-1250	4.0 MHz
1.8 V to 10 V	820 pF	33 pF	PS5CDLN-1303	3.5 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

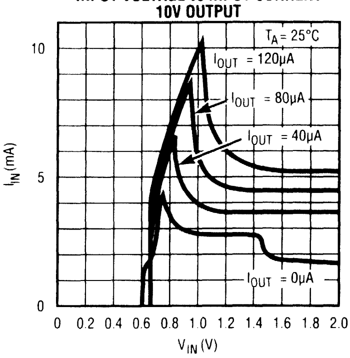
INPUT VOLTAGE vs OUTPUT VOLTAGE 10V OUTPUT



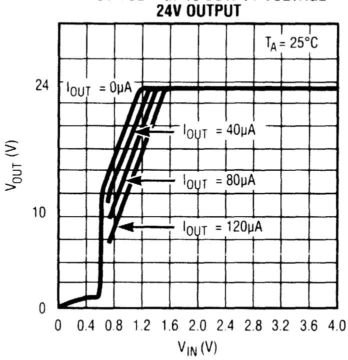
OUTPUT CURRENT vs OUTPUT VOLTAGE 10V OUTPUT



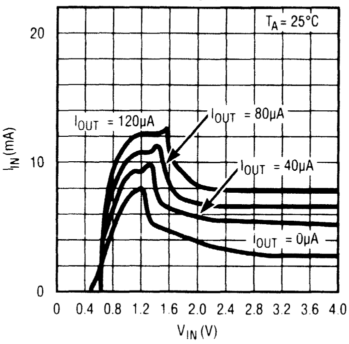
INPUT VOLTAGE vs INPUT CURRENT 10V OUTPUT



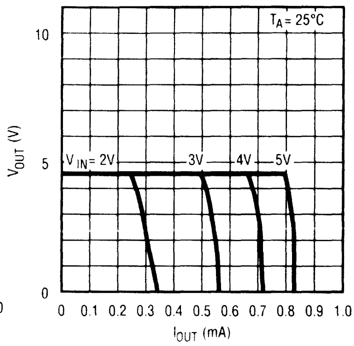
INPUT VOLTAGE vs OUTPUT VOLTAGE 24V OUTPUT



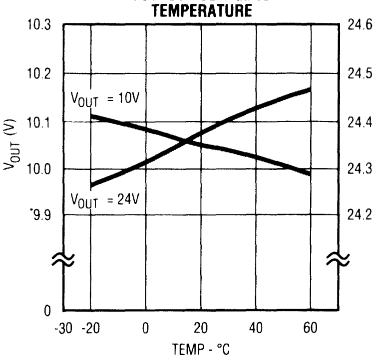
INPUT VOLTAGE vs INPUT CURRENT 24V OUTPUT



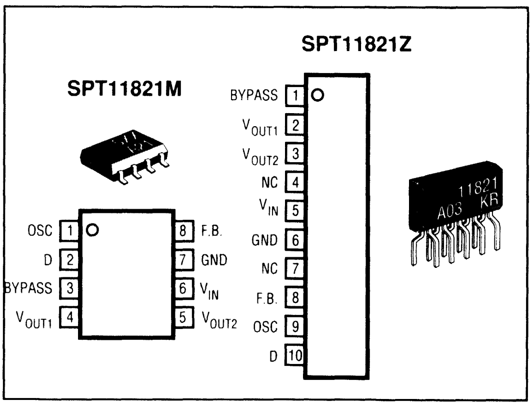
OUTPUT CURRENT vs OUTPUT VOLTAGE 24V OUTPUT



OUTPUT VOLTAGE vs TEMPERATURE



PIN ASSIGNMENT



SPT11821

8

SPT

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SIGNAL PROCESSING TECHNOLOGIES

EB100 EVALUATION BOARD

FEATURES

- 150 MSPS Nominal Conversion Rate
- 70 MHz Full Scale Input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- Clock Produced From Any Signal Generator
- Improved Output Drive (Doubly-Terminated 50 Ω)
- Optional Clock Divider Board Provided

APPLICATIONS

- Evaluation of HADC77100 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-Conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB100 demo board is intended to show the performance of the HADC77100 flash A/D converter and the HDAC10181A/B or HDAC54100 ultra-high speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board as shown in the block diagram below.

The HADC77100A/B is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a minimum 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

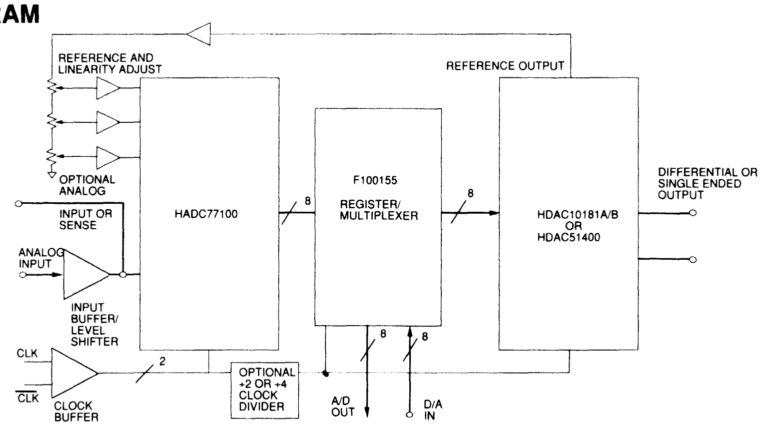
The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have optional video controls and can directly drive doubly-terminated 50 or 75 Ω loads to standard composite video levels. The DACs have internal references to supply themselves and the HADC77100 with stable voltage references and gain controls for different output voltage swings.

The HCMP96870 is a high speed differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50 Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2 V, +5 V, and ±12 to ±15 Volt power supplies are required for operation of the EB100 with nominal power dissipation of less than 10 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications.

9

BLOCK DIAGRAM



SIGNAL PROCESSING TECHNOLOGIES

EB101 EVALUATION BOARD

FEATURES

- 150 MSPS Nominal Conversion Rate
- 70 MHz Full Scale Input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable With Three Reference Ladder Taps)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- ECL Clock Produced From Any Signal Generator

APPLICATIONS

- Evaluation of HADC77200 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB101 demo board is intended to show the performance of the HADC77200 flash A/D converter and the HDAC10181 or HDAC54100 video D/A converters. Therefore, the board provides for the ADC or DAC to be tested together or separately.

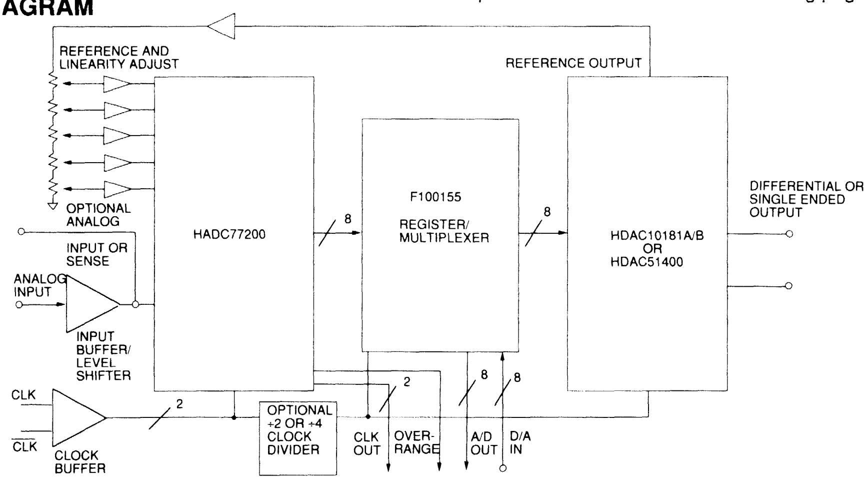
The HADC77200 is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have optional video controls and can directly drive doubly-terminated 50 or 75 Ω loads to standard composite video levels. The DACs have internal references to supply themselves and the HADC77200s with stable voltage references and gain controls for different output voltage swings.

The HCMP96870 is a high speed differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50 Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2 V, +5 V, and ±12 to ±15 Volt power supplies are required for operation of the EB101, with nominal power dissipation of less than 11 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications and is explained in more detail on the following pages.

BLOCK DIAGRAM



9

EB103 EVALUATION BOARD

SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- 400 MSPS Nominal Conversion Rate
- 100 to 150 MHz Full Scale Input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable With Three Reference Ladder Taps)
- Preamp Comparator Design/Optional Input Buffer
- ECL Timing Skew Clock Generator
- Improved D/A Output Drive, Doubly Terminated 50 Ω

APPLICATIONS

- Evaluation of HADC77200 A/D Converters
- Evaluation of HDAC51400 D/A Converters
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-Conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

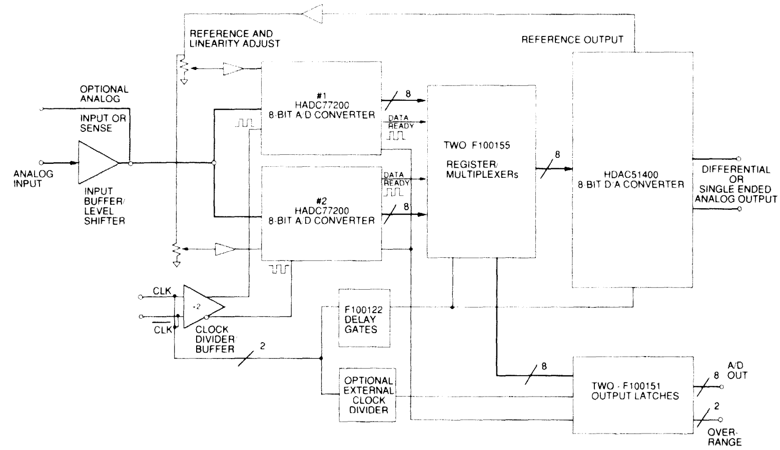
The EB103 demo board is intended to show the performance of the HADC77200 flash A/D converters in a ping-ponged mode, and the HDAC51400 ultra high speed D/A converter for reconstruction. Included on the unit are two 100K ECL multiplexers for combining the ping-ponged A/D converters' 16 bits of output data into 8 bits at twice the speed. The high speed data is routed between the A/D and D/A, and also off the board as full speed or as divided down data (external clock) for slower speed FFT measurements. This is shown in the block diagram below.

The HADC77200 is a monolithic, 8-bit flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 100 MHz at a 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HDAC51400 is a monolithic 8-bit D/A converter capable of converting data at rates of 400 MWPS. The part has optional video controls and can directly drive doubly-terminated 50 or 75 Ω loads to standard composite video levels. The DAC has an internal reference to supply itself and the HADC77200 with a stable voltage reference. It also has gain control to provide different output voltage swings so it can be used as a standard voltage output DAC.

The HCMP96870 is a dual high speed differential voltage comparator used to generate an adjustable ECL compatible clock signal for timing skew between the two A/D converters and D/A converter.

BLOCK DIAGRAM



9

SPT
SIGNAL PROCESSING TECHNOLOGIES

EB104 EVALUATION BOARD

FEATURES

- Provides Operating Environment for HADC574Z or HADC674Z and HDAC7545A Devices
- Fully Demonstrates Device Function and Resolution
- Eliminates Noisy Breadboard Evaluation Circuitry
- Buffered A/D and D/A Conversion Data Buses
- Includes Sample/Hold-Amp and Output Op Amp ICs
- Unipolar or Bipolar Operation

APPLICATIONS

- Evaluation/Comparison of HADC574/674Z Converters
- Evaluation/Comparison of HDAC7545A Converters
- System Development
- Data Acquisition Systems
- Bus Structured Instumentation
- Process Control Systems

GENERAL DESCRIPTION

The EB104 evaluation board fully demonstrates the capabilities of the HADC574/674Z and HDAC7545A 12-bit data conversion products. All of the basic power supply connections, control lines, and external components are included. The board can operate in an analog input/output fashion utilizing both A/D and D/A devices, or the devices can be operated separately. Unlike most laboratory breadboarding, the ground-planed PC board provides the necessary low-noise environment essential for 12-bit resolution. The board makes full use of connectors to allow easy hookup and operation.

Other support provided on the EB104 includes an input sample/hold amplifier, output operational amplifiers and potentiometers for offset and gain adjustments. Customization and function selections are performed by jumper pins. When considering the HDAC7545A for system design, the EB104 evaluation board provides a flexible, high performance evaluation vehicle.

The EB104 is supplied with an HADC574ZBCJ and an HDAC7545AACD. It will support all 574/674 and 7545 type devices.

BLOCK DIAGRAM

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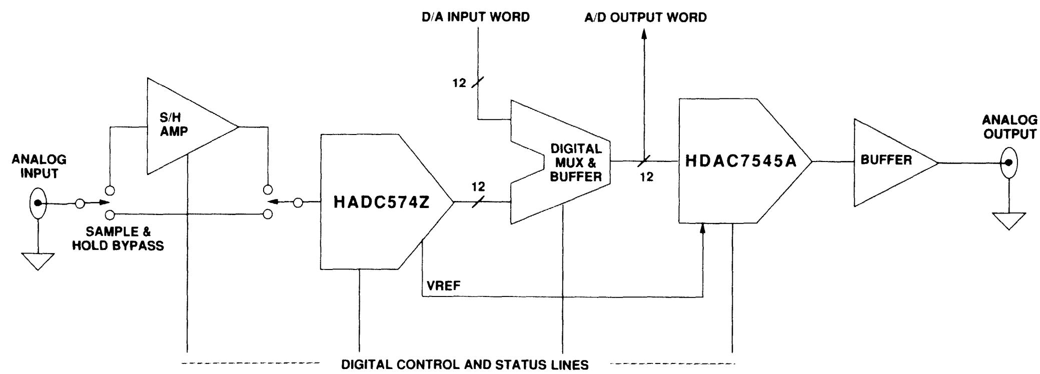


SIGNAL PROCESSING TECHNOLOGIES

EB105 EVALUATION BOARD

FEATURES

- Complete With Socketed HSCF24040 Device
- Demonstrates HSCF24040 Performance and Capabilities
- Toggle Switches For On-Board Control and Programming
- Connectors Allow Easy Interfacing of External Control, Programming, and Analog Signals
- Crystal Time Base
- Leaded Power Supply Connector

APPLICATIONS

- HSCF24040 Evaluation
- Prototype System Development
- Programmable General Purpose Subassembly

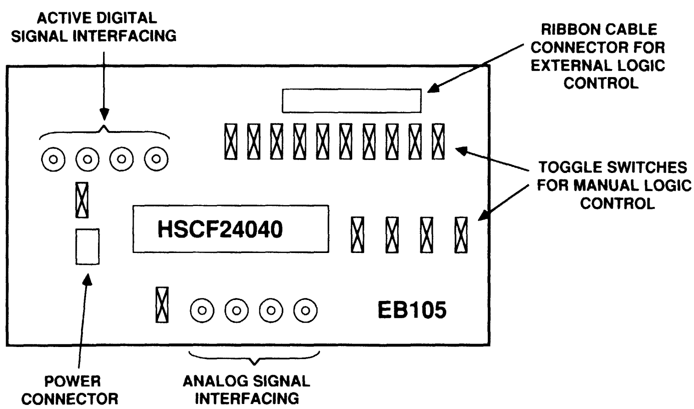
GENERAL DESCRIPTION

The EB105 evaluation board allows full exercise of the HSCF24040 programmable 7th order low pass active filter. Unlike a hand-wired breadboard, this ground-planed, printed circuit board provides a high performance, noise-free environment. It provides full demonstration and evaluation of the superb HSCF24040 dynamic characteristics. Programming and control of the device is conveniently enabled by on-board toggle switches. Alternately, programming and control can be accomplished through the on-board ribbon cable connector. This option allows software control which can aid in system development.

By making full use of the HSCF24040, the EB105 provides an analog input and output for both the RC and switched-capacitor filters. Both of these low-pass filters are fully programmable. Analog interfacing is accomplished with on-board BNC connectors to minimize noise and digital signal coupling. The EB105 also makes use of separate analog and digital supply grounds to further minimize digital coupling.

A clock crystal is supplied on the board which utilizes the HSCF24040 crystal oscillator feature. An external time base can be used optionally. BNC connectors are provided for external clock input and clock output for the CONVERT output and the SYNC control line. Use of BNC connectors on these active digital lines assures a minimum of digital-to-analog coupling.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7810/14 EVALUATION BOARD

FEATURES

- 20 and 40 MSPS Conversion Rates
- On-Board Reconstruction DAC
- Differential Clock Driver
- Data Output and Strobe Signal - ECL
- Data Output and Strobe Signal - TTL
- User Selectable Capture Clock

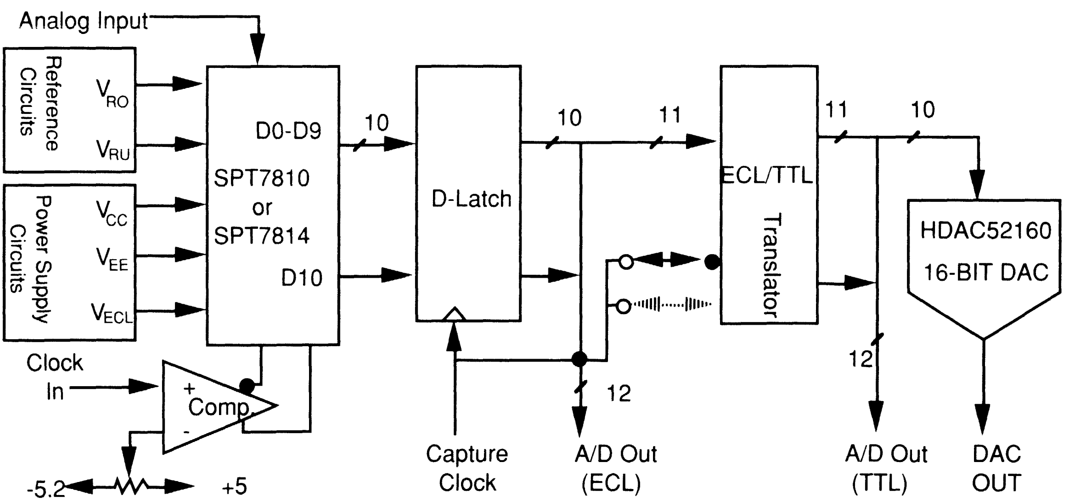
APPLICATIONS

- Evaluation of SPT7810 and SPT7814, 10 Bit ADC
- Engineering System Prototype Aid
- Incoming Inspection Tool
- AC Accuracy Testing: SNR, THD
- Power Supply Sensitivity Testing

GENERAL DESCRIPTION

The EB7810/14 evaluation board is intended to demonstrate the performance of the SPT7810/14, monolithic high speed analog-to-digital converters (ADC). The SPT7810 is capable of digitizing a ±2 V analog input signal up to 10 MHz into 10-bit words at a minimum of 20 MSPS update rate, while the SPT7814 is capable of digitizing at a minimum of 40 MSPS update rate.

BLOCK DIAGRAM



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EB7910/12 EVALUATION BOARD

SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- 10 and 20 MSPS Conversion Rate
- On-Board Reconstruction DAC
- Differential Clock Driver
- Data Output and Strobe Signal - ECL
- Data Output and Strobe Signal - TTL
- User Selectable Capture Clock
- On Board Reference Drivers
- On Board Power Supplies to SPT7910/12

APPLICATIONS

- Evaluation of SPT7910 and SPT7912
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Power Supply Sensitivity Testing
- Guide for the System Layout

GENERAL DESCRIPTION

The EB7910/12 Evaluation Board is intended to demonstrate the performance of the SPT7910 and SPT7912, monolithic high speed analog to digital converter (ADC). Both SPT7910 and SPT7912 have an analog input range of ±2V. The SPT7910 is capable of digitizing an analog input signal up to 5 MHz into 12-bit words at a minimum of 10 MSPS update rate, while the SPT7912 is capable of digitizing an analog input signal up to 10 MHz into 12-bit words at a minimum of 20 MSPS update rate.

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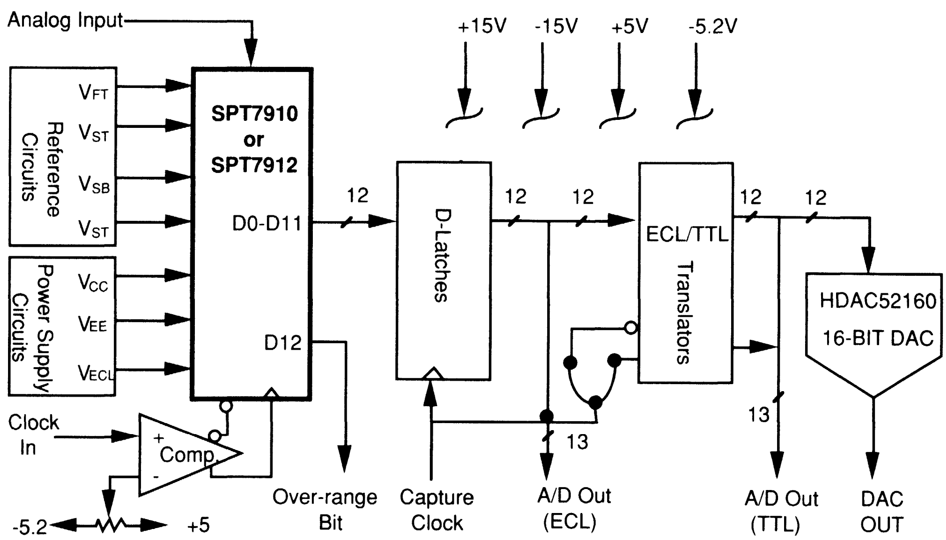
BLOCK DIAGRAM



SIGNAL PROCESSING TECHNOLOGIES

EB7820/24 EVALUATION BOARD

FEATURES

- 20 and 40 MSPS Conversion Rate
- On-Board Reconstruction DAC
- On Board Reference Drivers
- On Board Power Supplies to SPT7820/24
- Data Output- TTL
- User Selectable Capture Clock
- Improved Output Drive (Doubly-Terminated 50 Ω)

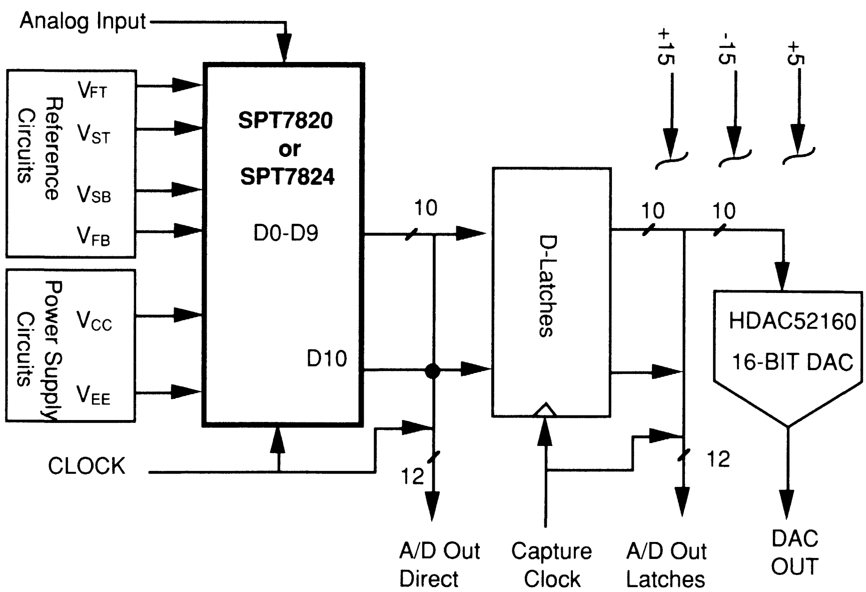
APPLICATIONS

- Evaluation of SPT7820 and SPT7824
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Power Supply Sensitivity Testing
- Guide for the System Lay-Out

GENERAL DESCRIPTION

The EB7820/24 Evaluation Board is intended to demonstrate the performance of the SPT7820 and SPT7824, monolithic high speed analog to digital converter (ADC). Both the SPT7820 and the SPT7824 have an analog input range of ±2 V. The SPT7820 is capable of digitizing an analog input signal up to 10 MHz into 10-bit words at a minimum of 20 MSPS update rate, while the SPT7824 is capable of digitizing an analog input signal at a minimum of 40 MSPS update rate.

BLOCK DIAGRAM



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EB7920/22 EVALUATION BOARD

SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- 10 and 20 MSPS Conversion Rate
- On-Board Reconstruction DAC
- On Board Reference Drivers
- On Board Power Supplies to SPT7920/22
- Data Output- TTL
- User Selectable Capture Clock

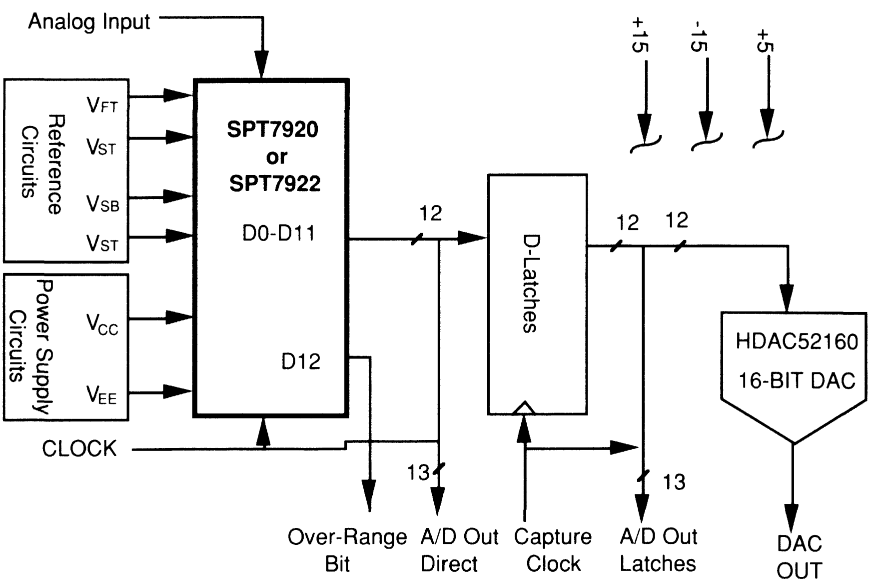
APPLICATIONS

- Evaluation of SPT7920 and SPT7922
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Power Supply Sensitivity Testing
- Guide for the System Lay-Out

GENERAL DESCRIPTION

The EB7920/22 Evaluation Board is intended to demonstrate the performance of the SPT7920 and SPT7922, monolithic high speed analog to digital converter (ADC). Both SPT7920 and SPT7922 have an analog input range of ±2 V. The SPT7920 is capable of digitizing an analog input signal up to 5 MHz into 12-bit words at a minimum of 10 MSPS update rate, while the SPT7922 is capable of digitizing an analog input signal up to 10 MHz into 12-bit words at a minimum of 20 MSPS update rate.

BLOCK DIAGRAM



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SPT

SIGNAL PROCESSING TECHNOLOGIES

APPLICATION NOTES & BRIEFS

CONTACT SPT FOR COMPLETE COPIES OF THE FOLLOWING APPLICATION NOTES.

AN100
EB100 EVALUATION BOARD

The EB100 Evaluation Board is used to show the performance of the HADC77100A/B flash ADC and HDAC10181A/B or HDAC51400 ultra-high speed DAC. The board provides for testing of the ADC and DAC either separately or together. Features include 150 MSPS minimum conversion rate, 70 MHz full scale input BW, and adjustable 1/2 LSB ILE. It is shipped fully assembled, calibrated and tested.

AN101
PARALLEL ANALOG-TO-DIGITAL CONVERTERS

A general overview of flash ADC architectures. Detailed application information for the HADC77100 and HADC77200, including product description, input structure, digital I/O, internal logic, clocking, specifications and testing.

AN102
EB101 EVALUATION BOARD

The EB101 Evaluation Board is used to show the performance of the HADC77200A/B flash ADC and HDAC10181A/B or HDAC51400 ultra-high speed DAC. The board provides for testing of the ADC and DAC either separately or together. Features include 150 MSPS minimum conversion rate, 70 MHz full scale input BW, and adjustable 1/2 LSB ILE. It is shipped fully assembled, calibrated and tested.

AN103
EB103 EVALUATION BOARD

The EB103 is used to show the performance of the HADC77200 in a ping-ponged mode, and the HDAC51400 ultra high speed DAC for reconstruction. Features include 400 MSPS nominal conversion rate, 100 to 150 MHz full scale input BW, and adjustable 1/2 LSB ILE with three reference ladder taps. The board is shipped fully assembled, calibrated and tested.

AN104
VIDEO DACS AND RASTER GRAPHICS

Explanation of high speed DACs and how they are used in CRT designs and raster graphics systems. Discussion of video DAC performance parameters including speed, rise time, glitch energy, resolution, logic compatibility and analog output drive. A block diagram and associated graphs are included to clearly illustrate raster scan graphics systems.

AN106
EB104 EVALUATION BOARD

The EB104 is used to demonstrate performance of the HADC574/674Z and HDAC7545A 12-bit data conversion products. The board can be used to evaluate the ADC and DAC either separately or together. The low noise environment provided by the board makes 12-bit resolution easier to achieve compared to most lab breadboarding. Features include buffered A/D and D/A conversion data buses, S/H amp and output op-amp ICs, and unipolar or bipolar operation. It is shipped fully assembled and tested.

AN108
THERMAL CONSIDERATIONS FOR HIGH PERFORMANCE DEVICES

General overview of the integrated circuit package and its interface to the outside world. Information on system thermodynamics, calculating the operating die temperature, package thermal resistance and heat sinking are included. Thermal resistances that need to be of concern to system designers are also discussed.

AN109
EB105 EVALUATION BOARD

The EB105 Evaluation Board provides for the full demonstration and evaluation of the HSCF24040 programmable 7th order low pass active filter. Programming and control of the device is enabled by on-board toggle switches. The board provides a ground-planed, high performance, noise free environment for testing of the device. It is shipped fully assembled and tested with one HSCF24040.

AN7810/14
EB7810/14 EVALUATION BOARD

The EB7810/14 Evaluation Board is used to demonstrate the performance of the SPT7810 and SPT7814. Features include reference inputs, clock driver circuit, on-board reconstruction DAC, data output and strobe signals for ECL & TTL, user selectable capture clock, and conversion rates up to 40 MSPS. Detailed discussions on power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization is included. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, and power supply sensitivity testing. The board is shipped calibrated and tested. The ADC device in not included with the board.

AN7820/24
EB7820/24 EVALUATION BOARD

The EB7820/24 Evaluation Board is used to demonstrate the performance of the SPT7820 and SPT7824. Features include on-board reference drivers, on-board reconstruction DAC, TTL data output, user selectable capture clock, and conversion rates up to 40 MSPS. Detailed discussions on power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization is included. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, and power supply sensitivity testing. The board is shipped calibrated and tested. The ADC device in not included with the board.

AN7910/12
EB7910/12 EVALUATION BOARD

The EB7910/12 Evaluation Board is used to demonstrate the performance of the SPT7910 and SPT7912. Features include on-board reference drivers, on-board reconstruction DAC, data output and strobe signals for ECL and TTL, user selectable capture clock, and conversion rates up to 20 MSPS. Detailed discussions on power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization is included. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, power supply sensitivity testing and as a guide for system layout. The board is shipped calibrated and tested. The ADC device is not included with the board.

AN7920/22
EB7920/22 EVALUATION BOARD

The EB7920/22 Evaluation Board is used to demonstrate the performance of the SPT7920 and SPT7922. Features include on-board reference drivers, on-board reconstruction DAC, TTL data output, user selectable capture clock, and conversion rates up to 20 MSPS. Detailed discussions on power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization is included. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, power supply sensitivity testing and as a guide for system layout.. The board is shipped calibrated and tested. The ADC device is not included with the board.

AN111
ANALOG/DIGITAL INTERFACE REQUIREMENTS FOR THE HSCF24040

Discussion of the internal workings of the HSCF24040 to assist the user in system design. Specific information on analog and digital interface requirements and how to choose proper SC and RC filter bandwidths. Excellent tool for understanding switched-cap filter basics and system design.

AB100
USING ECL DACS WITH TTL LOGIC

Discussion of why most high speed DACs are designed to perform in ECL systems because of speed and low noise characteristic of this logic group. Specific information on techniques to allow the SPT ECL DACs to be used in TTL systems. Other solutions to overcome perceived incompatibility between -5.2 V and +5 V are included.

AB102
CHARGE SCALING DATA CONVERTERS

Current scaling versus charge scaling in data conversion techniques are discussed. The SPT BI-CMOS process used to manufacture the HADC574Z and 674Z includes this technique to lower power consumption and provide an inherent S/H function. A simple explanation of how this is performed is included.

AB103
HADC574Z AND HADC674Z ANALOG INPUT STRUCTURE

Discussion of the BICMOS process and design architecture of the input circuits of the HADC574/674Z, and how it reduces the need for specific signal source characteristics and signal buffering. Brief discussion of conversion events and DC dynamic input characteristics of the device, and how the input structure improves the overall performance of the ADC.

AB104
TESTING THE HADC574/674Z ON THE LTS2020

Technical information on the LTS2020 test system commonly used as an incoming inspection tool is included. Hardware and software modifications to achieve accurate test results for the HADC574/674Z are explained.

AB105
GLITCH ENERGY IN HIGH SPEED D/A CONVERTERS

Brief explanation of how glitch energy affects some applications, how to overcome these problems, and why SPT devices have superior glitch performance. Specific information on SPT's DAC designs and defining glitch energy is included.

SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

SPT

SIGNAL PROCESSING TECHNOLOGIES

QUALITY ASSURANCE

QUALITY AND RELIABILITY

To remain competitive in today's integrated circuit market, a company must work continuously to improve quality. Improved quality and increased reliability are achieved by reducing variation of output using statistical process control.

Quality and reliability of electronic components are critical issues at Signal Processing Technologies. Realizing the relationship between its customers' success and its own, SPT has put into place a quality assurance program that makes its products among the highest quality and most reliable components available. In doing so, the SPT program complies with the following military specifications: MIL-STD-883, MIL-M-38510, MIL-I-45208, MIL-Q-9858, MIL-STD-105, MIL-STD-1686, and MIL-STD-45662.

Certification in accordance with MIL-STD-883 and MIL-M-38510 is required in order to manufacture and sell Class B and Hi-Rel products. SPT is certified in this area and updates the process annually by means of self audits and required document control. SPT's MIL-STD-883 manufacturing process includes:

- A dedicated facility where manufacturing and testing operations are performed with state-of-the-art instrumentation and automatic test equipment.
- Fully documented and controlled manufacturing processes that utilize procedures to ensure total compliance with applicable military and customer specifications.
- Screening operations designed to isolate potential infant mortality failures before they are shipped to customers.
- A documented product traveler system that details and guarantees flow of product throughout the SPT manufacturing process.
- A training program to assure that SPT employees with responsibilities in the manufacturing flow of products understand and adhere to the requirements of controlled specifications and procedures.
- Operator training and certification programs to provide highly trained personnel qualified to manufacture and test SPT parts.
- A product analysis system that provides the necessary input to update applicable processes and associated documentation.
- An SPT manufacturing facility that minimizes electrostatic discharge (ESD) damage. The SPT ESD program complies with guidelines established by MIL-STD-1686.
- Equipment calibration performed and controlled by the guidelines established under MIL-STD-45662.
- A quality assurance inspection system that maintains quality products acceptable to both the customer and SPT.
- Product reliability ensured through comprehensive Quality Assurance monitoring throughout the manufacturing process and screening of the final product.
- Initial full-product qualification for Class B and Hi-Rel products before the product is released into the production process.

All SPT products are fully characterized and initially qualified to MIL-M-38510 requirements before introduction to the production process. After successful product qualification, periodic product reliability testing and screening of Quality Conformance Inspection groups A, B, C, and D takes place to assure the short-term quality and long-term reliability of the products.

APPLICABLE GOVERNMENT SPECIFICATIONS AND STANDARDS

MIL-STD-883
TEST METHODS & PROCEDURES FOR MICROELECTRONICS

MIL-STD-883 establishes uniform methods, controls and procedures for designing, testing, identifying and certifying microelectronic devices, including basic environment tests. All certified SPT products are compliant with all applicable methods and associated procedures for Class B products.

MIL-M-38510
GENERAL SPECIFICATION FOR MICROCIRCUITS

MIL-M-38510 supports government microcircuit application and logistic programs. All certified SPT products are compliant with applicable sections of MIL-M-38510 as required by MIL-STD-883 for Class B related products.

MIL-I-45208
INSPECTION SYSTEM REQUIREMENTS

MIL-I-45208 establishes requirements for inspection systems pertaining to the inspections and tests necessary to substantiate product conformance to drawings, specifications and contract requirements, and to all inspections and tests required by the contract. SPT's inspection system meets the requirements of MIL-I-45208.

MIL-Q-9858
QUALITY PROGRAM REQUIREMENTS

MIL-Q-9858 establishes a contractor quality program to assure compliance with the requirements of applicable contracts. SPT's quality program meets the requirements of MIL-Q-9858.

MIL-STD-105
SAMPLING PROCEDURES & TABLES FOR INSPECTION BY ATTRIBUTE

MIL-STD-105 establishes sampling plans and procedures for inspection by attributes. SPT's sampling procedures and tables comply with the requirements of MIL-STD-105.

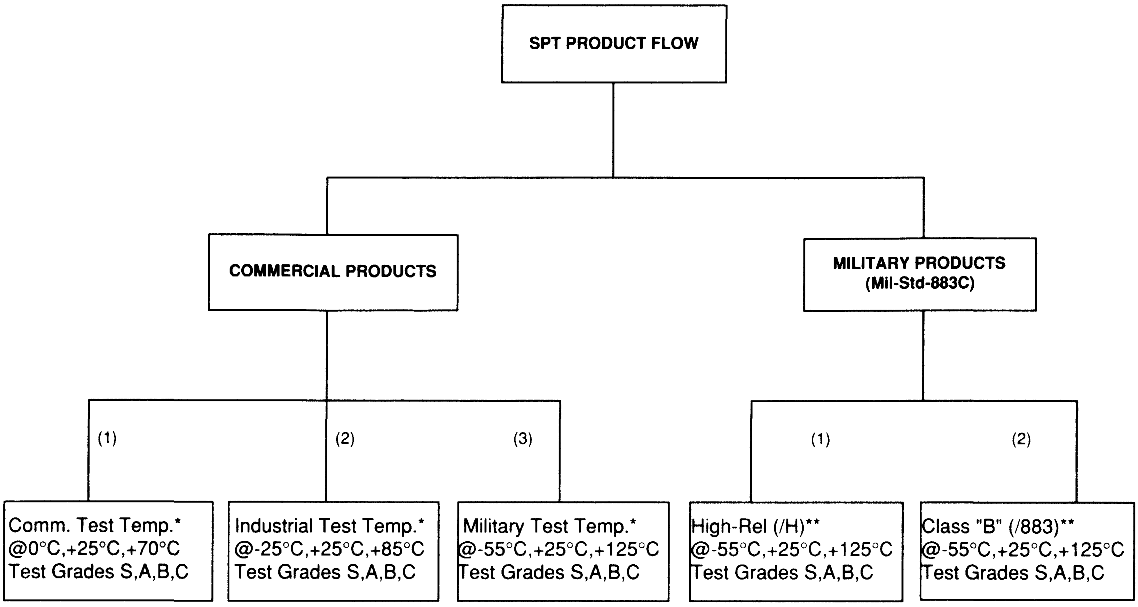
MIL-STD-1686
ELECTROSTATIC DISCHARGE CONTROL PROGRAM FOR PROTECTION OF ELECTRICAL AND ELECTRONIC PARTS, ASSEMBLIES AND EQUIPMENT

MIL-STD-1686 establishes the requirements for an ESD control program to minimize the effects of ESD on parts, assemblies, and equipment. An effective ESD program increases reliability while decreasing maintenance actions and lifetime costs. SPT's ESD program fully complies with the requirements of MIL-STD-1686.

MIL-STD-45662
CALIBRATION SYSTEMS REQUIREMENTS

MIL-STD-45662 provides requirements for the establishment and maintenance of a calibration system to control the accuracy of measurement and test equipment and measurement standards used to assure that supplies and services delivered to the government comply with prescribed technical requirements. SPT's calibration system was established to the requirements of MIL-STD-45662.

SPT PRODUCT FLOW DESCRIPTION



* The only difference between Commercial, Industrial, and Military is the Test temperature, although all three are considered Commercial products.

** Differences between	/H	/883
1) Mil-M-38510 Certified wafer FAB required.	No	Yes
2) Lot traceability required	Yes	Yes
3) PDA Calculation required	Yes	Yes
4) Off-shore assembly permitted	Yes	Yes
5) Method 5004, Class "B" screening procedures	Yes	Yes
6) Method 5005, Class "B" initial product Qual. group A, B, C, & D required	Yes	Yes

** Differences between	/H	/883
7) QCI Visual & Group A on every production lot required	Yes	Yes
8) QCI group B on every production lot required	No	Yes
9) QCI group C every 3 months of production required	No	Yes
10) QCI group D every 6 months of production required	No	Yes
11) Certificate of Compliance w/every lot shipment required	Yes	Yes

SPT COMMERCIAL PRODUCT FLOW (1)

COMMERCIAL BUILD	WAFER FABRICATION
AQL 0.65%	WAFER INCOMING INSP.
100%	WAFER PROBE, VISUAL, BAKE
100%	WAFER MOUNT, SAW, CLEAN, VIS.
AQL 0.65%	DIE VISUAL INSPECTION
100%	DIE ATTACH
100%	WIRE BOND, BOND PULL, VISUAL
AQL 1.50%	PRECAP VISUAL INSPECTION
100%	BAKE, SEAL
100%	TIN PLATE, INSPECTION
AQL 0.65%	GROSS LEAK
100%	LEAD TRIM, VISUAL
AQL 0.10%	PKG. INCOMING INSPECTION
DC TEST @ ROOM*100%	PKG. FINAL ELECT. TEST
100%	PKG. MARKING
EXTERNAL VISUAL INSP.,AQL 0.10% ELECT. TEST @ +25C, AQL 0.65%	QCI

COMMERCIAL DIE FLOW ENDS HERE

SPT QUALITY ASSURANCE PROCESS MONITORING & MANUFACTURING AUDIT

(1) INCLUDES COMMERCIAL, INDUSTRIAL & MILITARY TEST TEMPERATURE. THIS STANDARD FLOW IS SUBJECT TO CHANGE DUE TO PRODUCT SPECIFIC FLOW.

* HOT AND/OR COLD TEST TEMPERATURES AND AC TEST ARE PERFORMED ONLY WHEN REQUIRED.

SPT MILITARY PRODUCT FLOW (1)

(Mil-Std-883C)

Mil-M-38510 Compliance	WAFER FABRICATION
AQL 0.40%	WAFER INCOMING INSP.
100%	WAFER PROBE, VISUAL, BAKE
100%	WAFER MOUNT, SAW, CLEAN, VISUAL
AQL 0.40%	DIE VISUAL INSPECTION
100%	DIE ATTACH
100%	WIRE BOND, BOND PULL, DIE SHEAR, VISUAL
Method 2010, Cond. B, AQL 0.65%	PRECAP VISUAL INSP.
100%	BAKE, SEAL
Method 1008, Cond. C, 100%	STABILIZATION BAKE
Method 1010, Cond.C or Method 1011, Cond. A 100%	TEMP CYCLE OR THERM. SHOCK
Method 2001, Cond. E 100%	CONSTANT ACCELERATION (CENTRIFUGE)
100%	LEAD TRIM, SOLD. DIP INSPECTION
Method 1014 100%	FINE & GROSS LEAK,INSP.
LTPD=2	PKG./INCOMING INSP.
DC Test @ +25°C 100%	PRE B/I ELECT. TEST
Method 1015, 160 hrs. @125°C 100%	BURN-IN
DC Test @-55°C,+25°C,+125°C & AC Test @ +25°C 100%	PKG., FINAL ELECT. TEST
100%	PKG. MARKING
External Visual Insp., Method 2009 LTPD=2 & Method 5005	QCI*

MILITARY DIE FLOW ENDS HERE (arrow points between DIE VISUAL INSPECTION and DIE ATTACH)

SPT QUALITY ASSURANCE PROCESS MONITORING & MANUFACTURING AUDIT (bracket covering WAFER FABRICATION through QCI*)

(1) INCLUDES HIGH-REL (/H) AND CLASS "B" (/883) PRODUCTS. THIS STANDARD FLOW IS SUBJECT TO CHANGE DUE TO PRODUCT SPECIFIC FLOW.

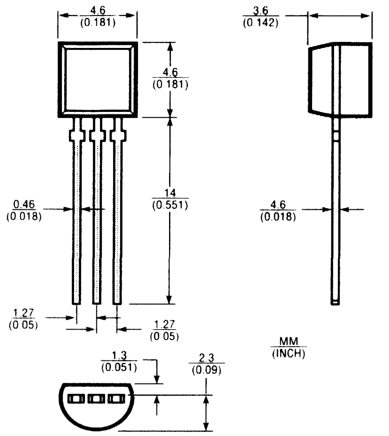
* GROUP "A" SAMPLE ELECTRICAL TEST IS PERFORMED @-55°C, +25°C, +125°C FOR DC, AND @ 25°C FOR AC FOR BOTH /H AND /883 PRODUCTS.

SIGNAL PROCESSING TECHNOLOGIES

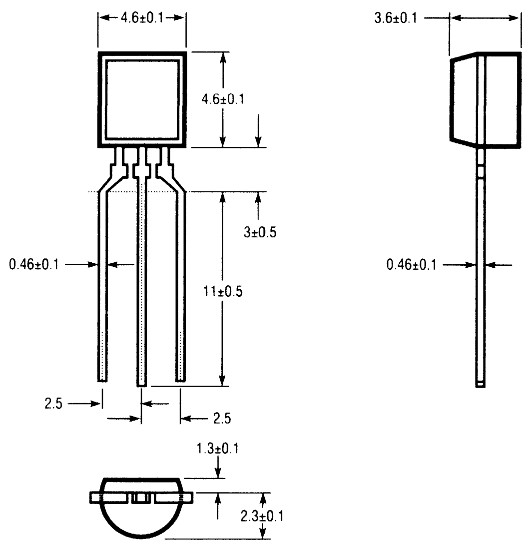
EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING

PACKAGING INFORMATION

3-LEAD PLASTIC TO-92N



3-LEAD PLASTIC TO-92NT



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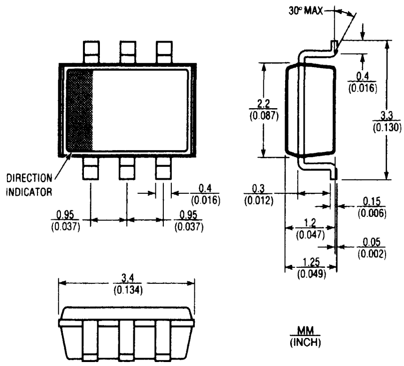
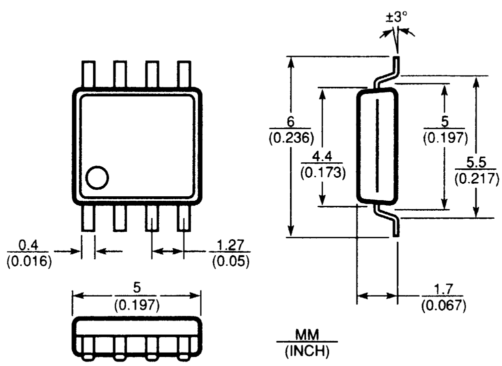
6-LEAD PLASTIC



8-LEAD PLASTIC



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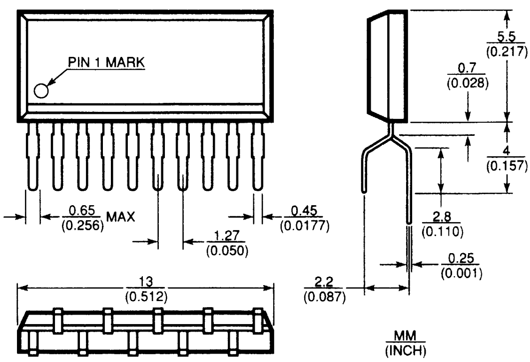

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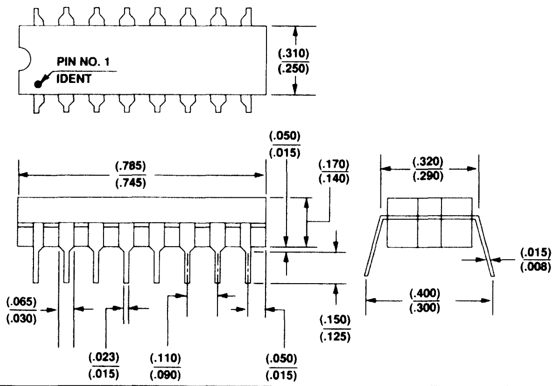

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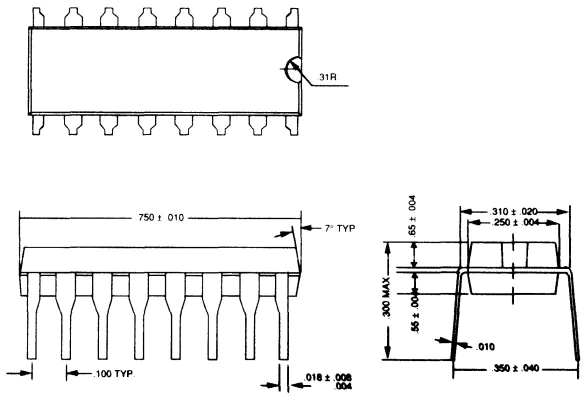

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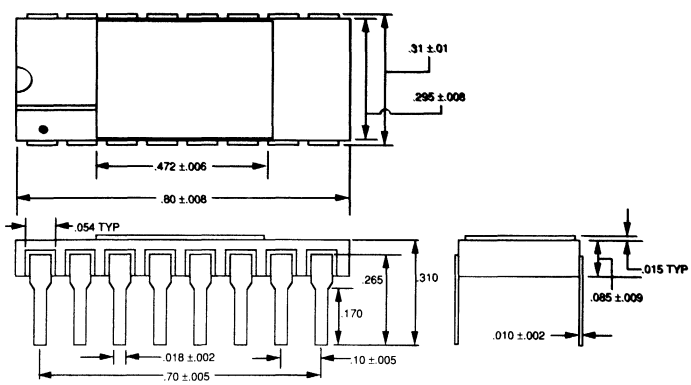

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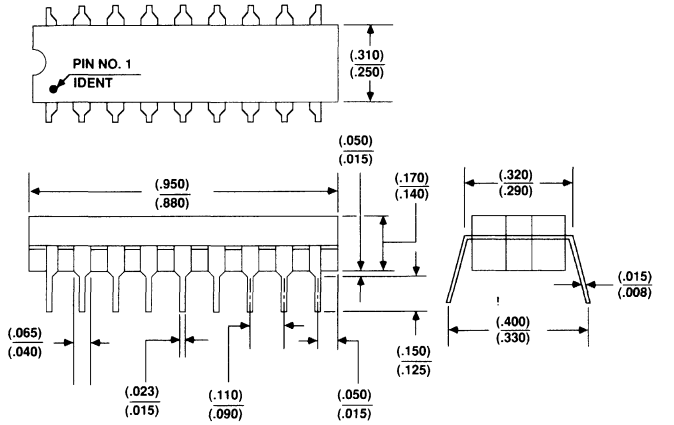

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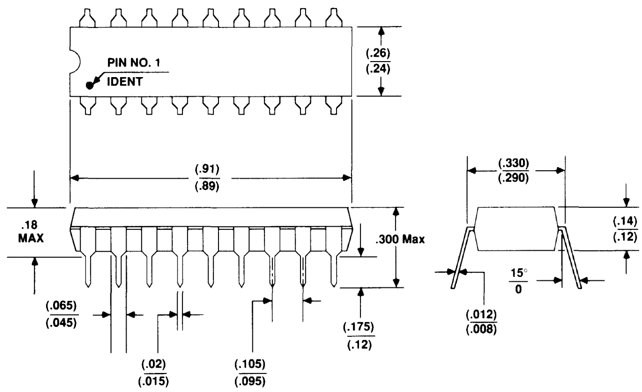

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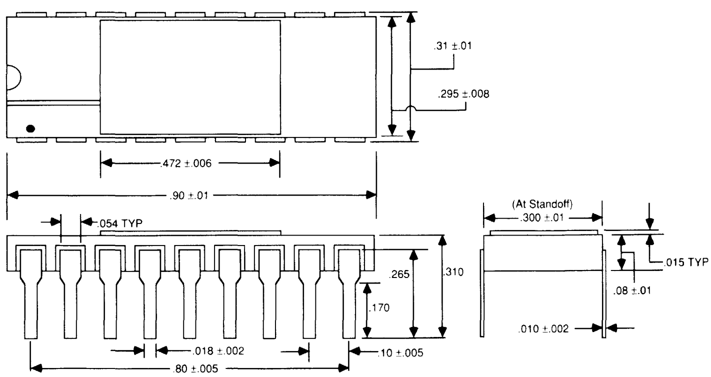

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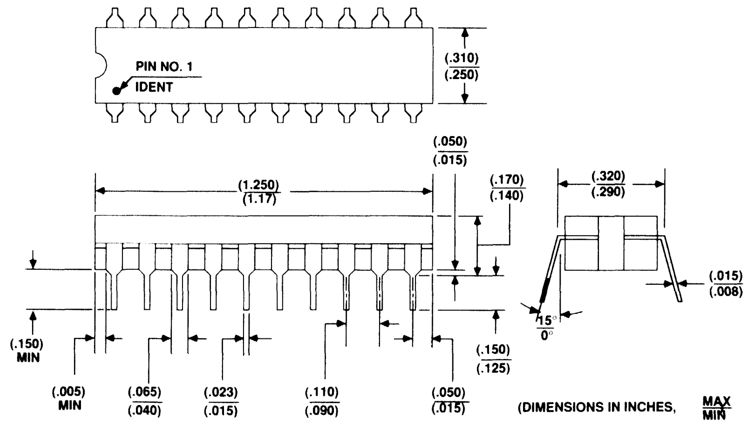

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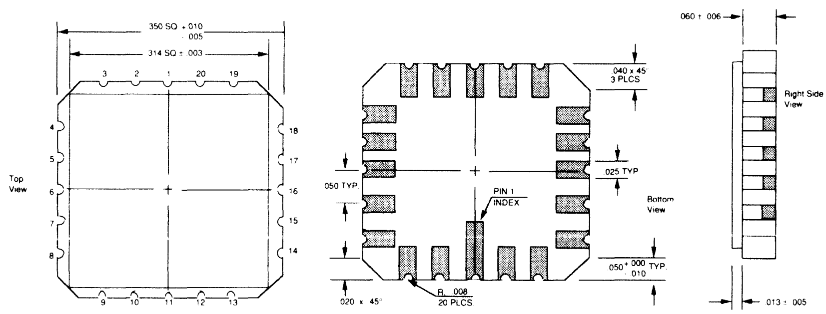

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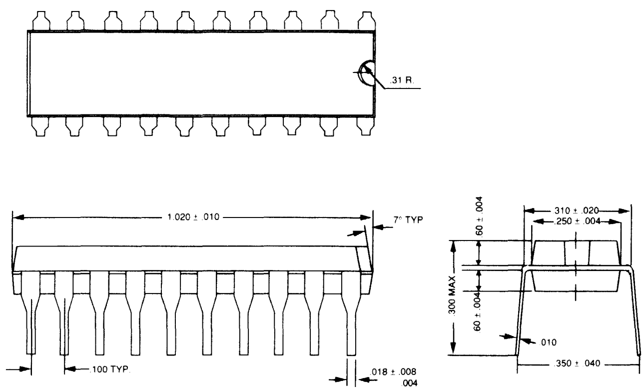

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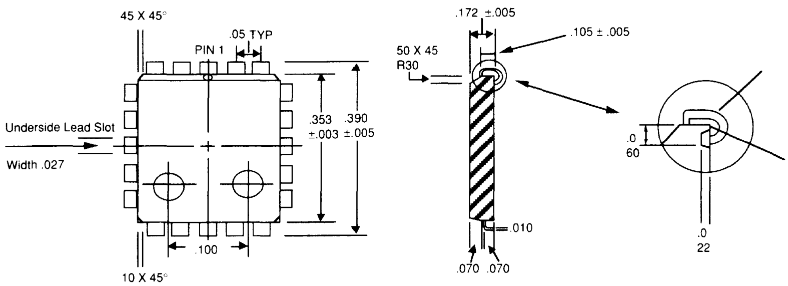

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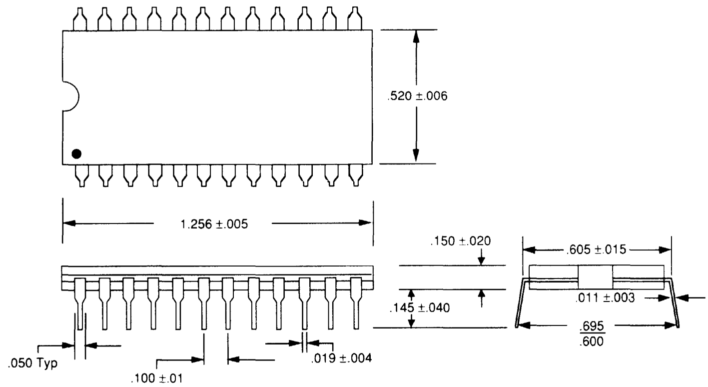

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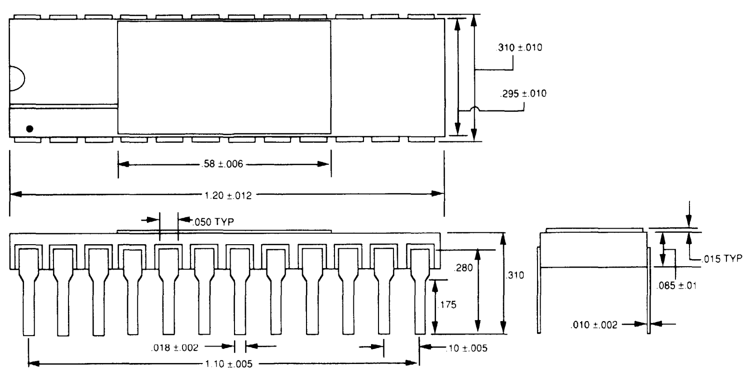

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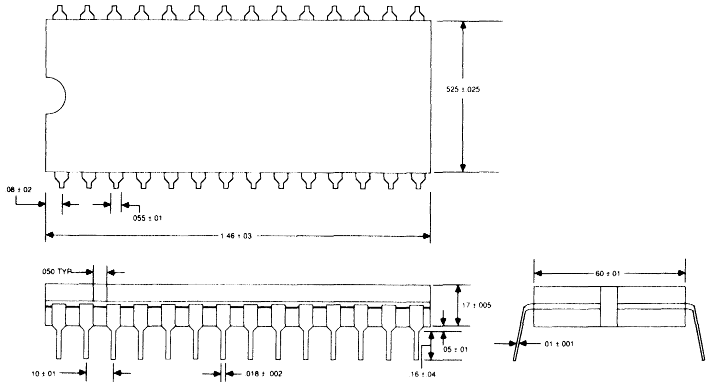

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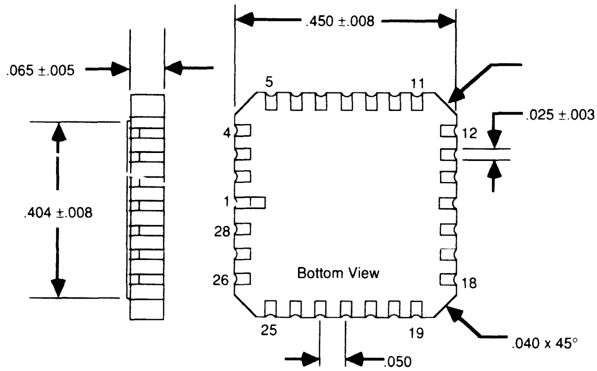

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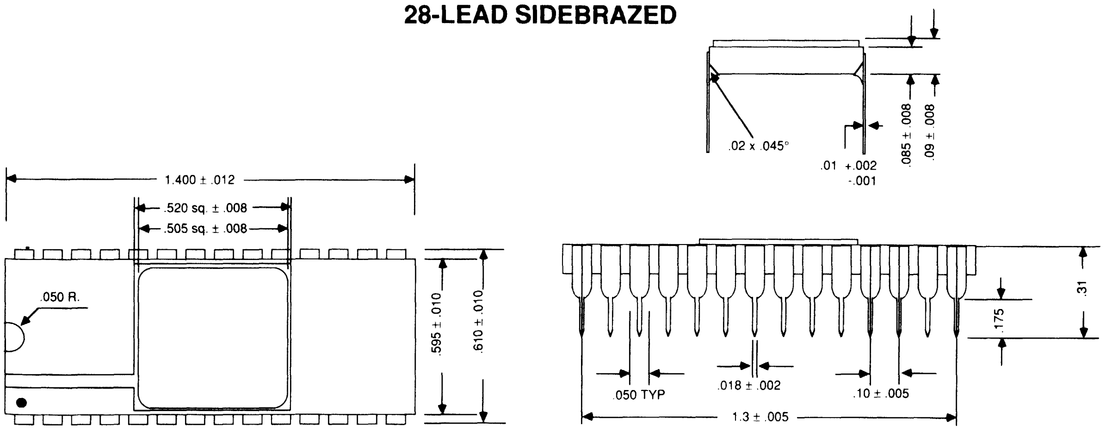

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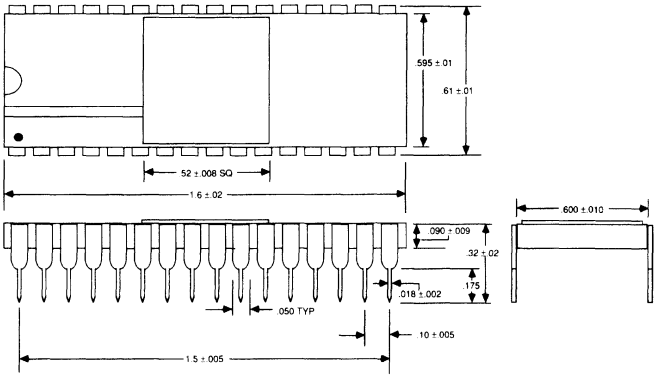

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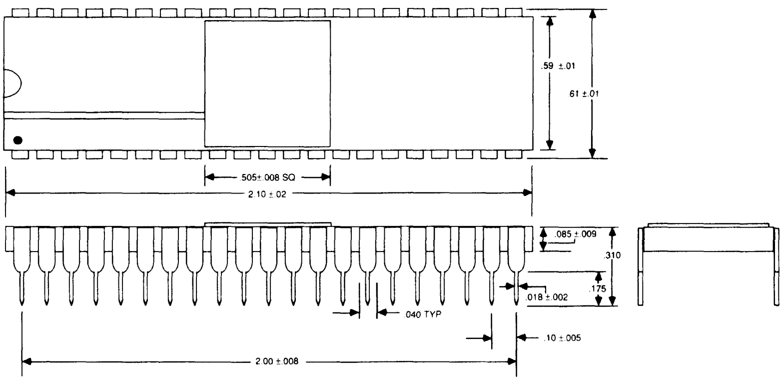

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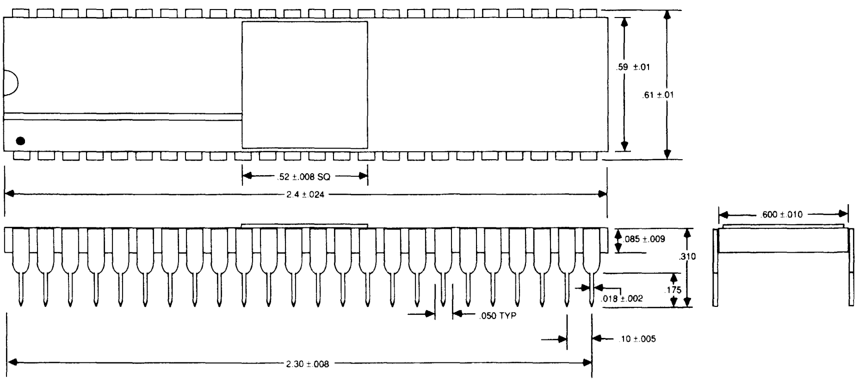

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SIGNAL PROCESSING TECHNOLOGIES

EXCELLENCE IN DATA CONVERSION AND SIGNAL PROCESSING